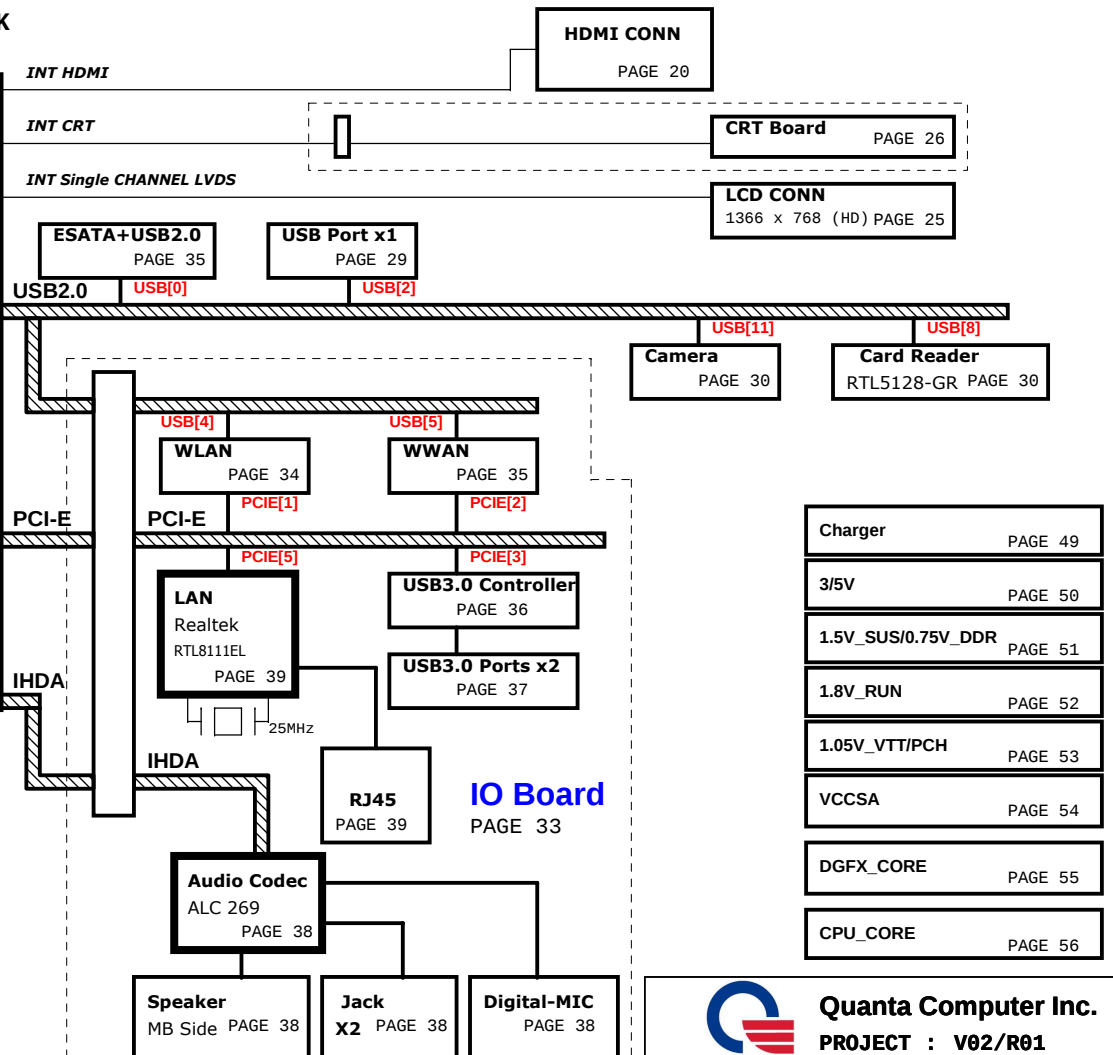


V02/R01 UMA BLOCK DIAGRAM

The diagram illustrates the system architecture of the Intel Atom Z870. At the top, the **CPU** (Sandy Bridge 35W, PGA 988) is connected to two **DDRIII-SODIMM** memory modules (DDRIII 1333 MT/s) via **FDI LINK** (2.56T /s) and **DMI LINK** (2.56T /s). The CPU is also connected to the **PCH** (Mobile Intel Series 6 Chipset, HM67 Cougar Point, BGA 989, 25 mm X 25 mm) via **IGFX Interfaces**. The PCH is connected to the **KBC** (KBC ITE 8518, PAGE 32) via **LPC**. The KBC is connected to the **FAN & Thermal** sensor (PAGE 45) and the **SPI ROM 512KB** (PAGE 41). The PCH is also connected to the **SPI ROM 4MB** (PAGE 41) via **SPI**. The PCH is connected to the **E-SATA** (PAGE 28), **SATA -HDD** (PAGE 31), and **ODD** (PAGE 36) via **SATA4 3G /S**, **SATA0 6G /S**, and **SATA1 6G /S** respectively. The PCH is also connected to the **3-axis Fall Sensor** (PAGE 31) via **SMBUS**. The PCH is connected to the **onn.** (PAGE 42) via **onn.** (PAGE 42). The PCH is also connected to the **25MHz** and **32.768KHz** oscillators.

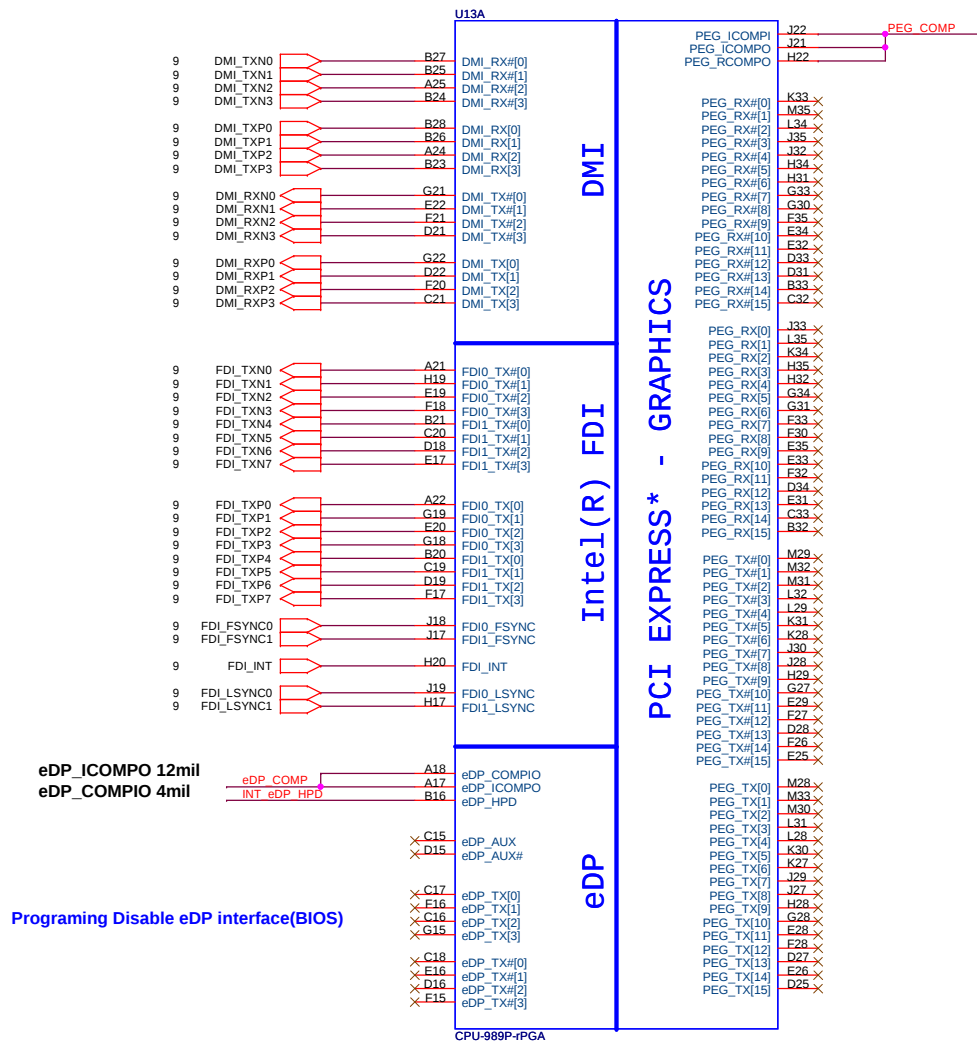


power State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					

SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								

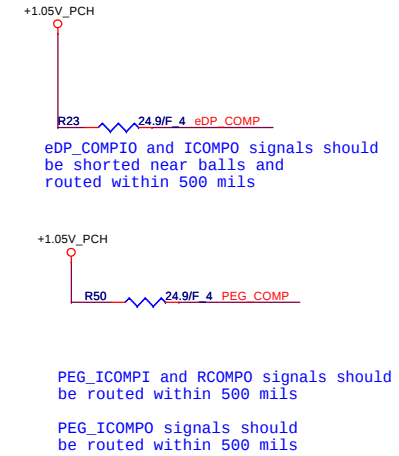


Sandy Bridge Processor (DMI, PEG, FDI)

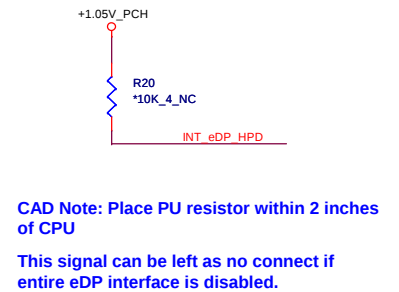


PEG_ICOMPO 12mil
PEG_ICOMPIO, PEG_RCOMPIO 4mil,

DP & PEG Compensation

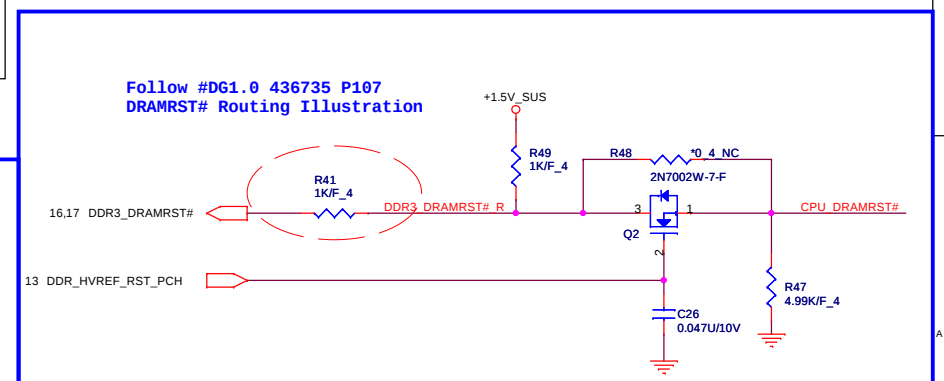
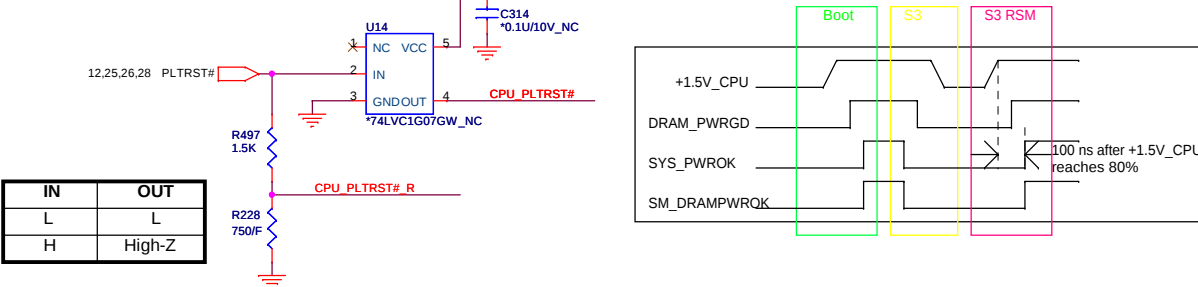
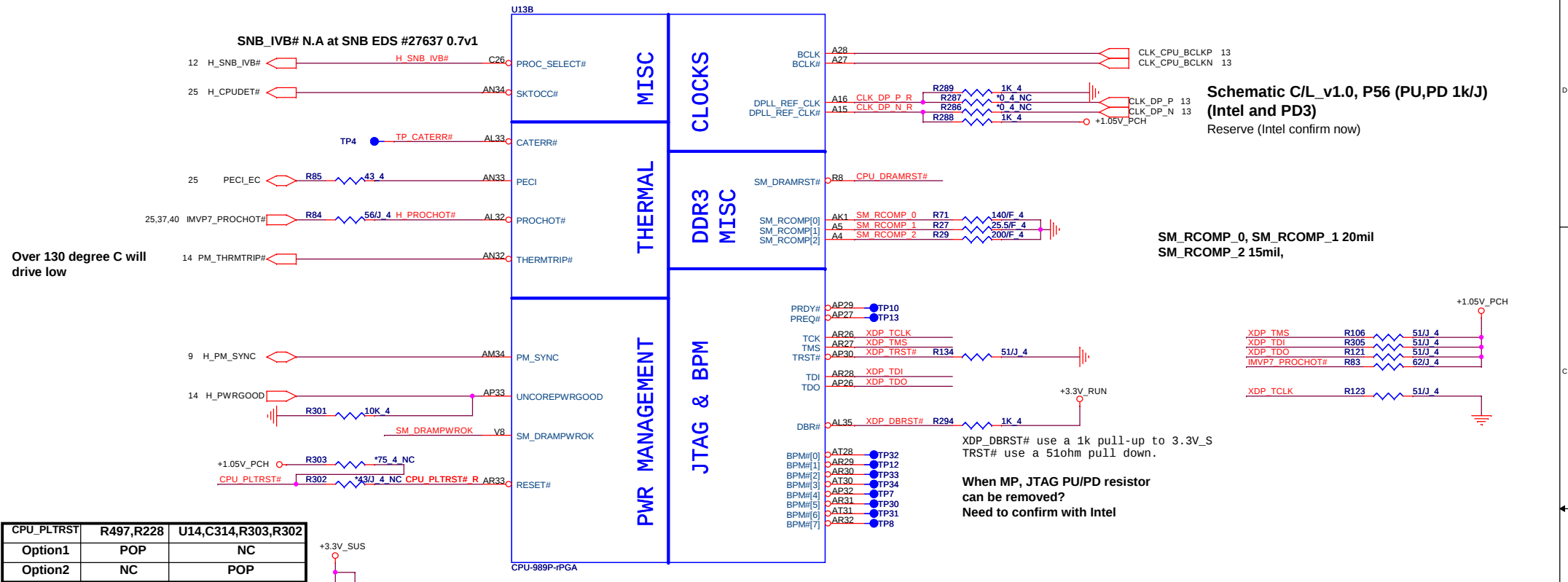


eDP Hot-plug (Disable)

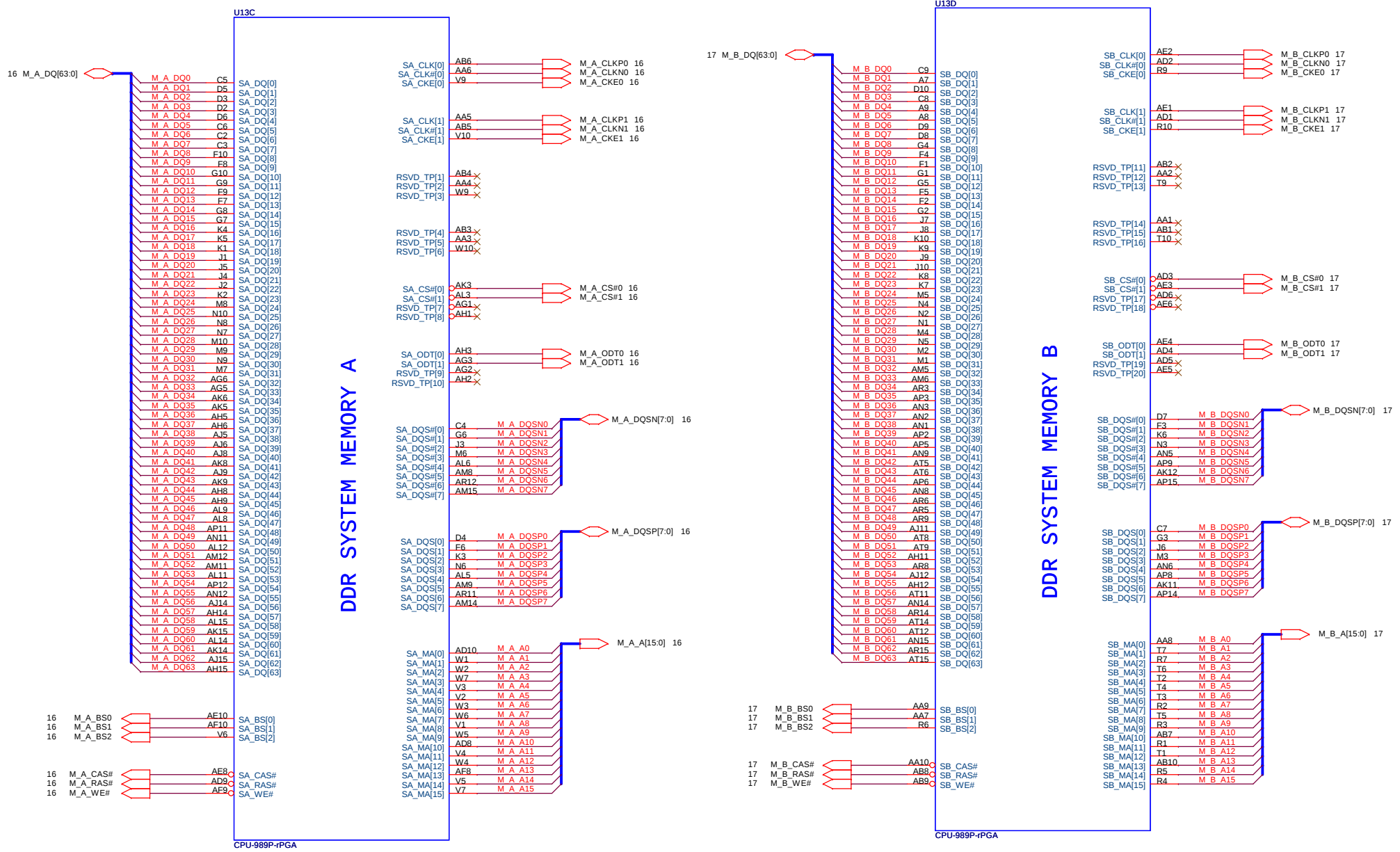


Programming Disable eDP interface(BIOS)

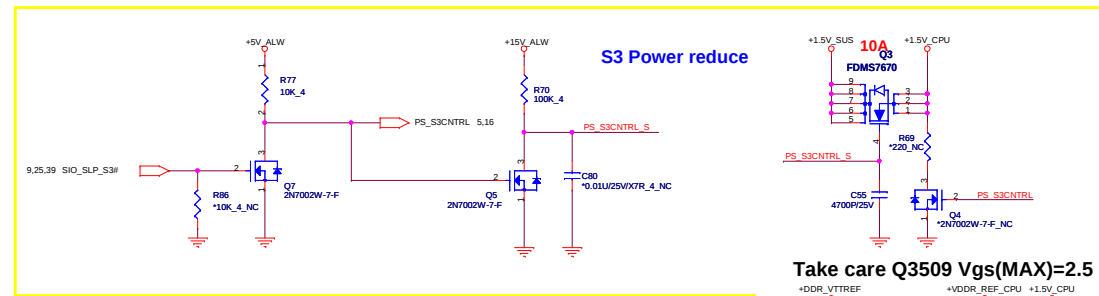
Sandy Bridge Processor (CLK, MISC, JTAG)



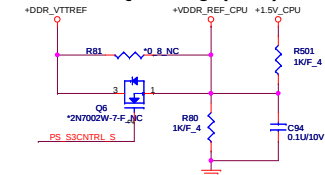
Sandy Bridge Processor (DDR3)



	2	
Sandy Bridge Processor (GRAPHIC POWER)		



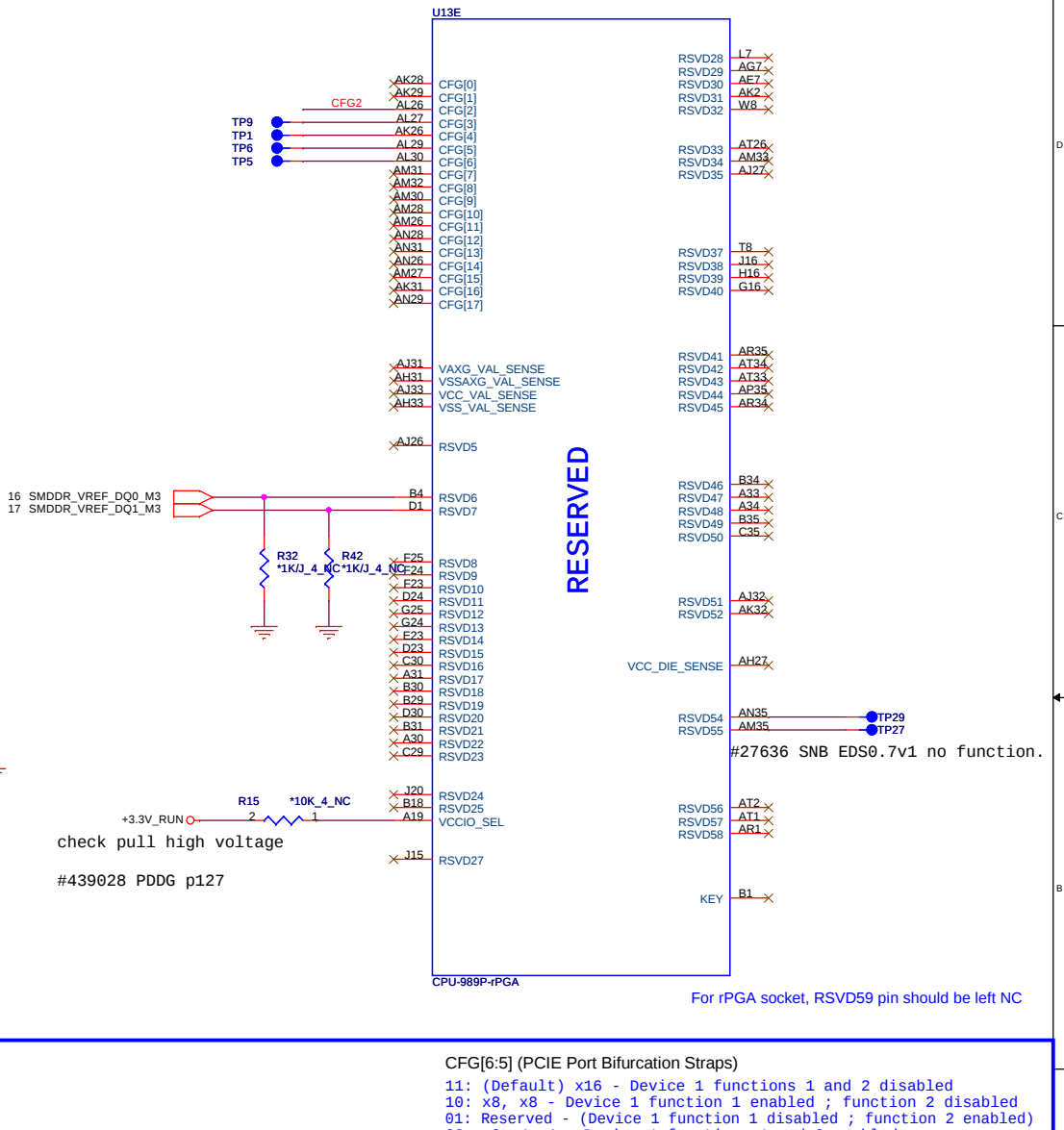
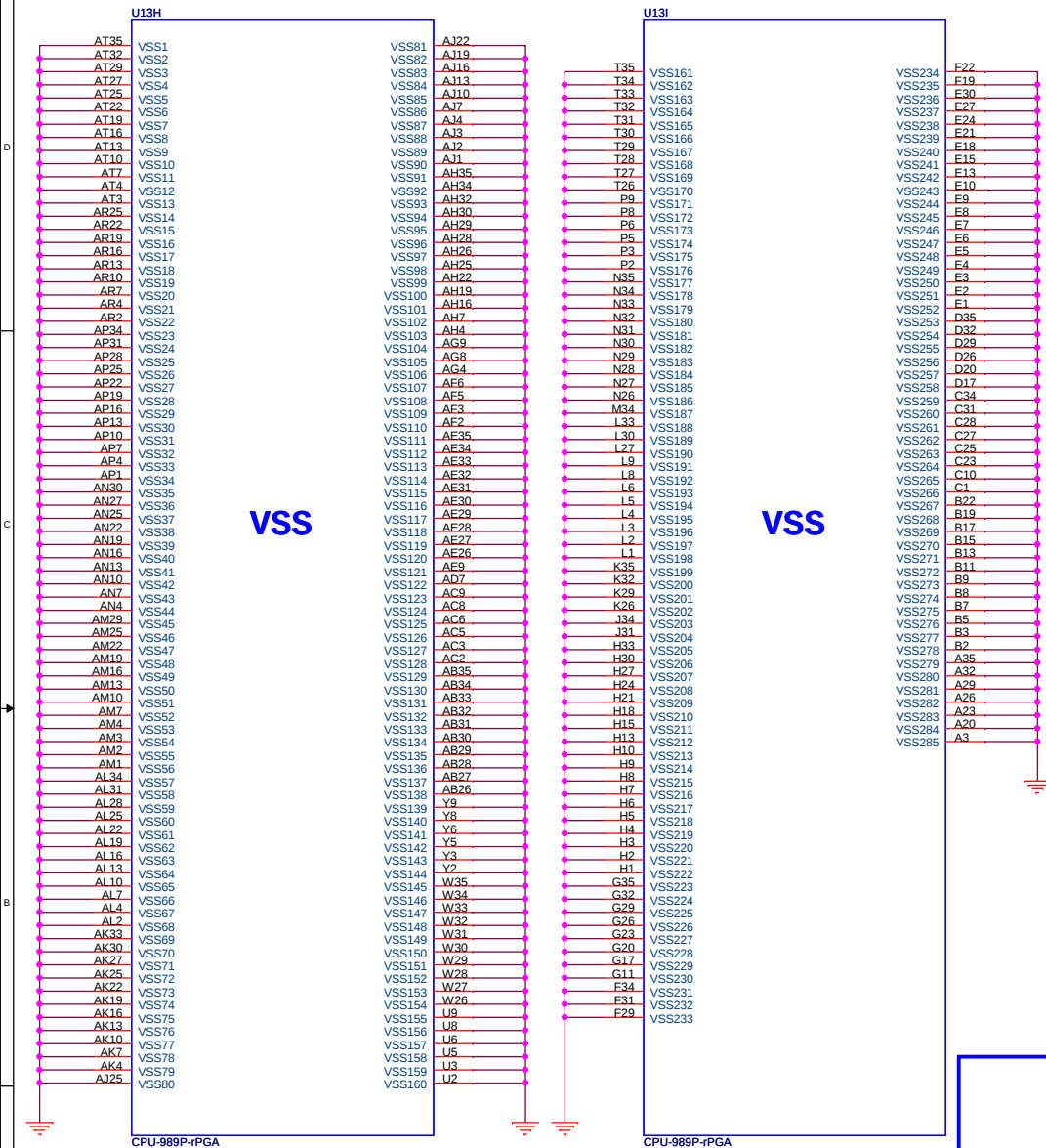
Take care Q3509 $V_{gs}(\text{MAX})=2.5$



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Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)



For rPGA socket, RSVD59 pin should be left NC

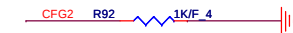
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

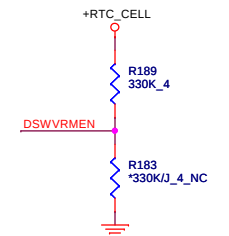
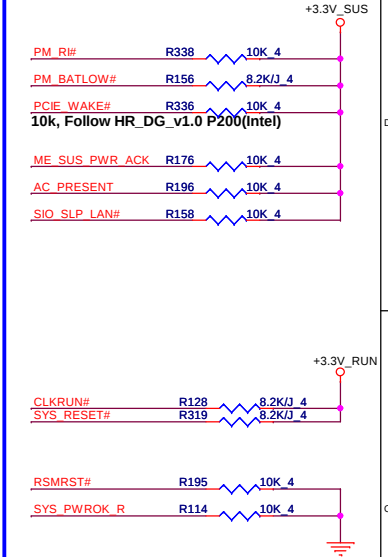
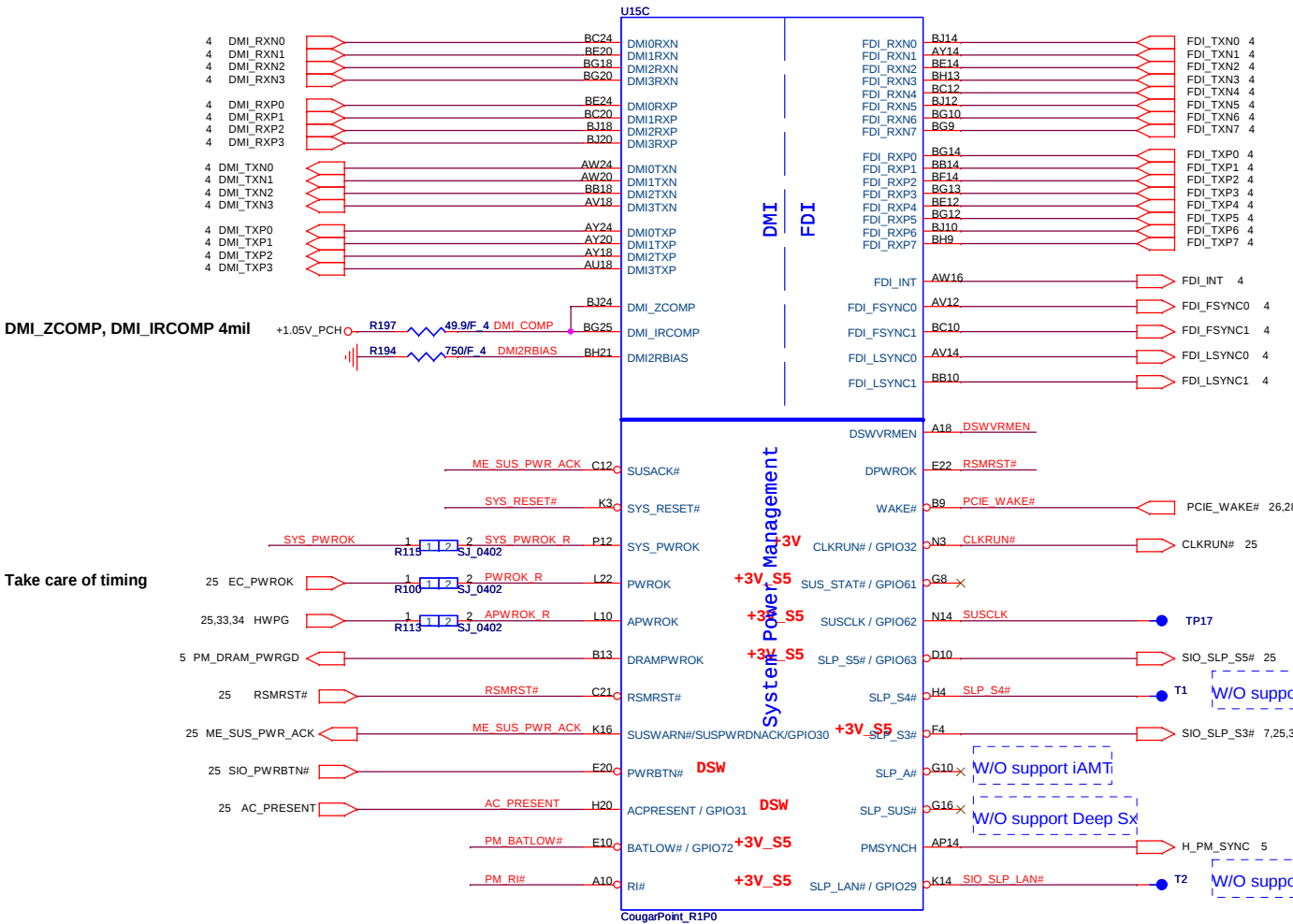
The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

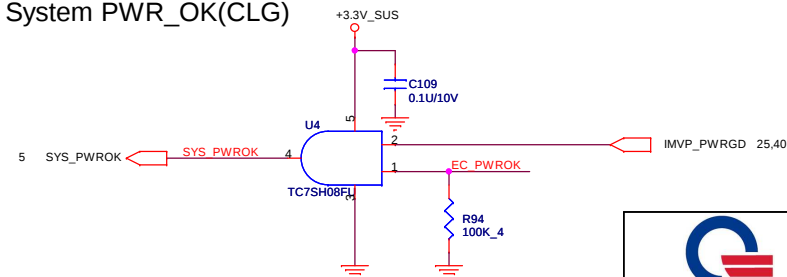


Cougar Point (DMI, FDI, PM)

PCH Pull-high/low(CLG)



System PWR_OK(CLG)

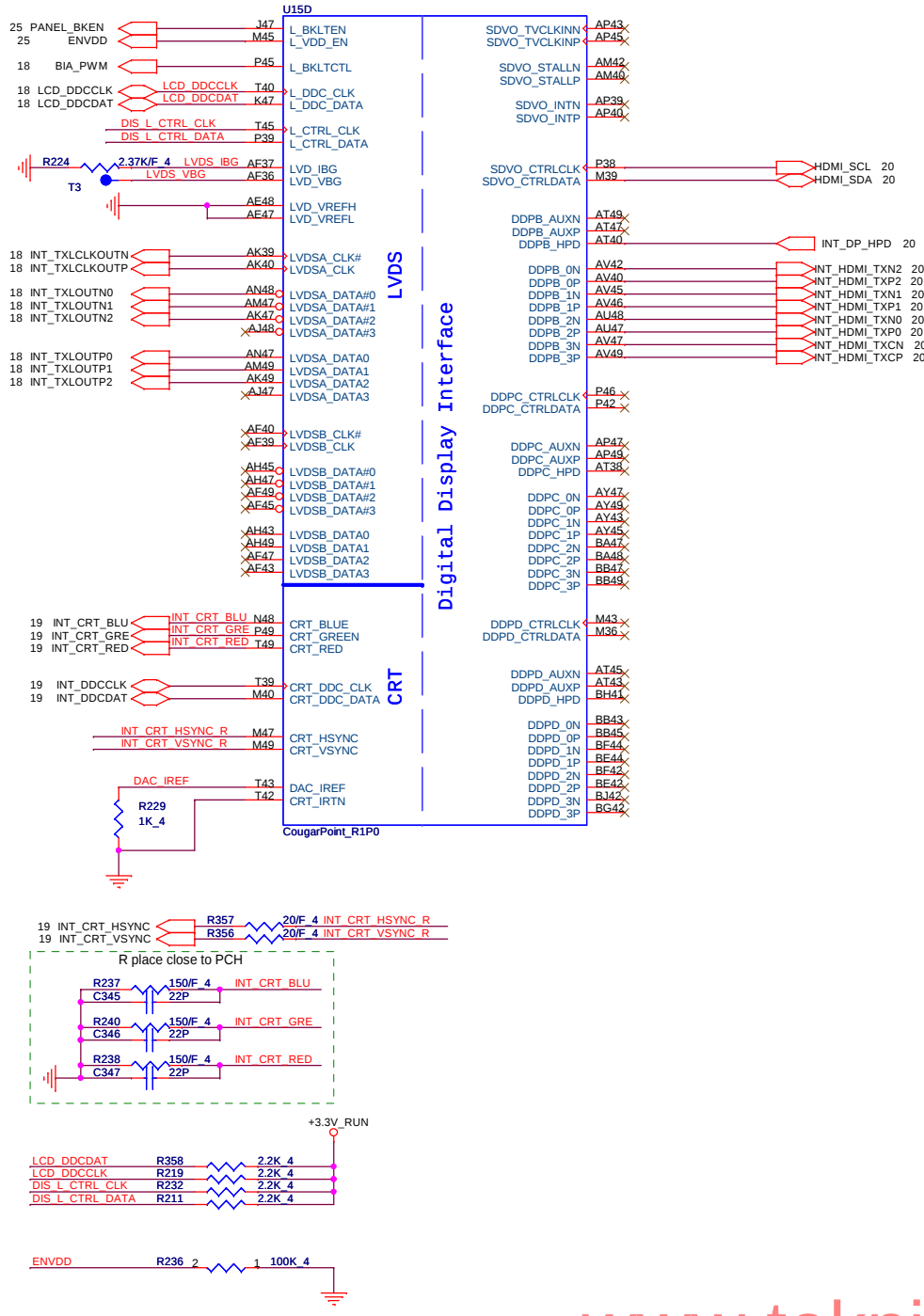


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PROJECT : V02/R01

Size	Document Number	Rev
	Cougar Point 1/7	1A
Date:	Wednesday, January 19, 2011	Sheet 9 of 51

Cougar Point (LVDS,DDI)

Cougar Point (GND)



INT_HDMI

CougarPoint_R1P0

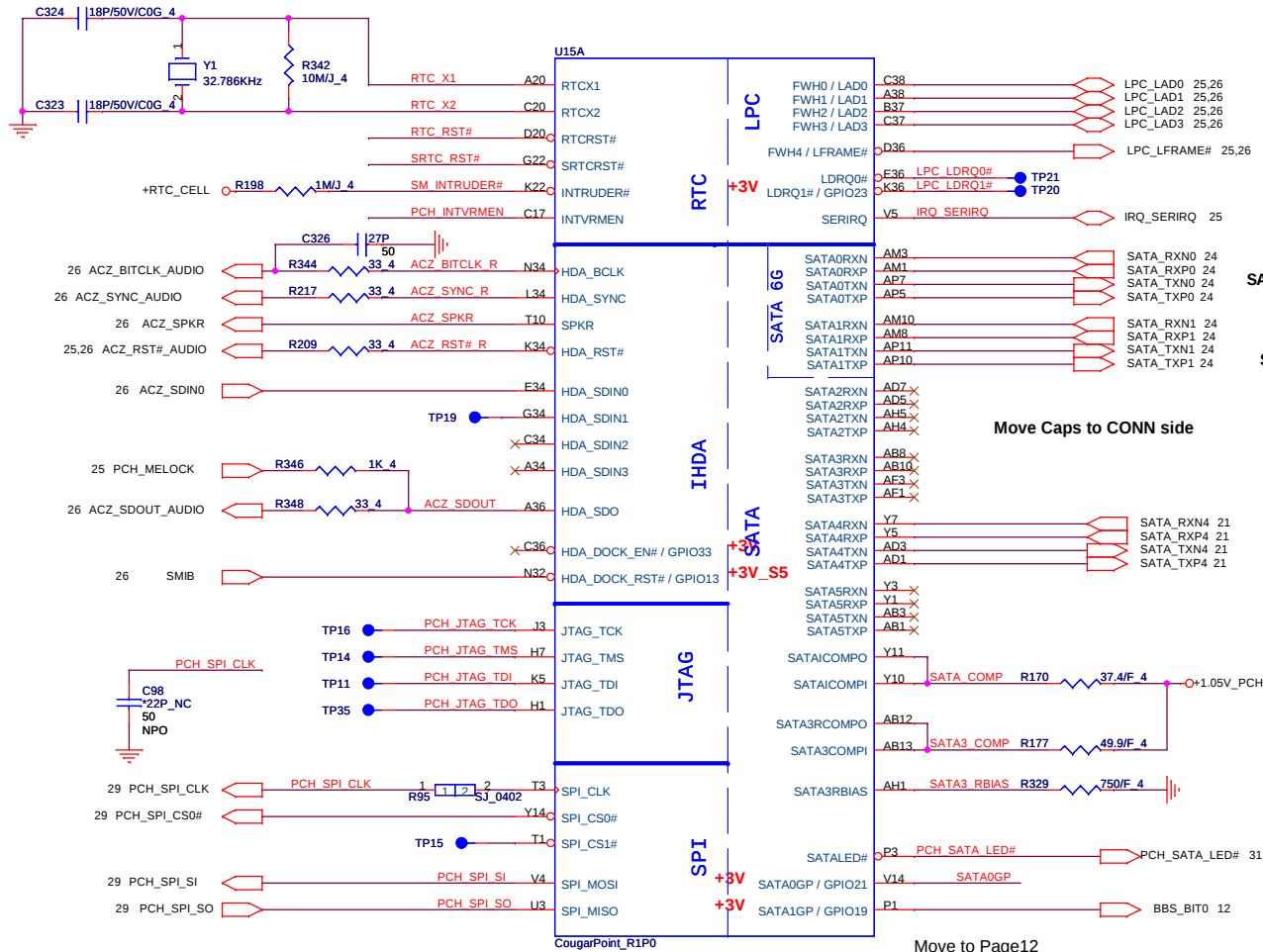


Quanta Computer Inc.

PROJECT : V02/R01

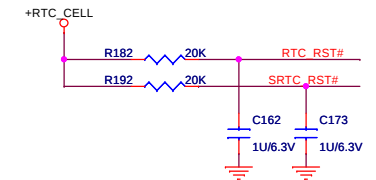
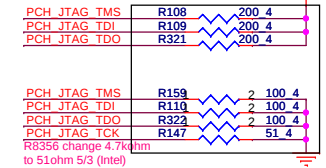
Size	Document Number	Rev
	Cougar Point 2/7	1A
Date:	Wednesday, January 19, 2011	Sheet 10 of 51

Cougar Point (HDA, JTAG, SATA)



PCH JTAG Debug (CLG)

5% fine (Intel), 210->200 (PDDG, Intel) MP remove(Intel) +3.3V_SUS



SATA HDD/SSD

SATA ODD

ESATA

Move Caps to CONN side

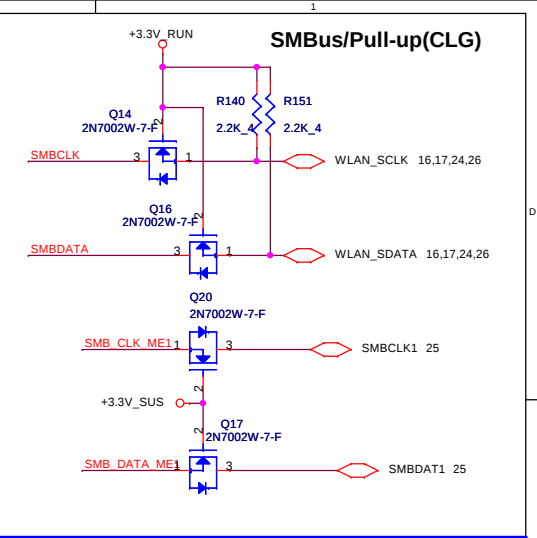
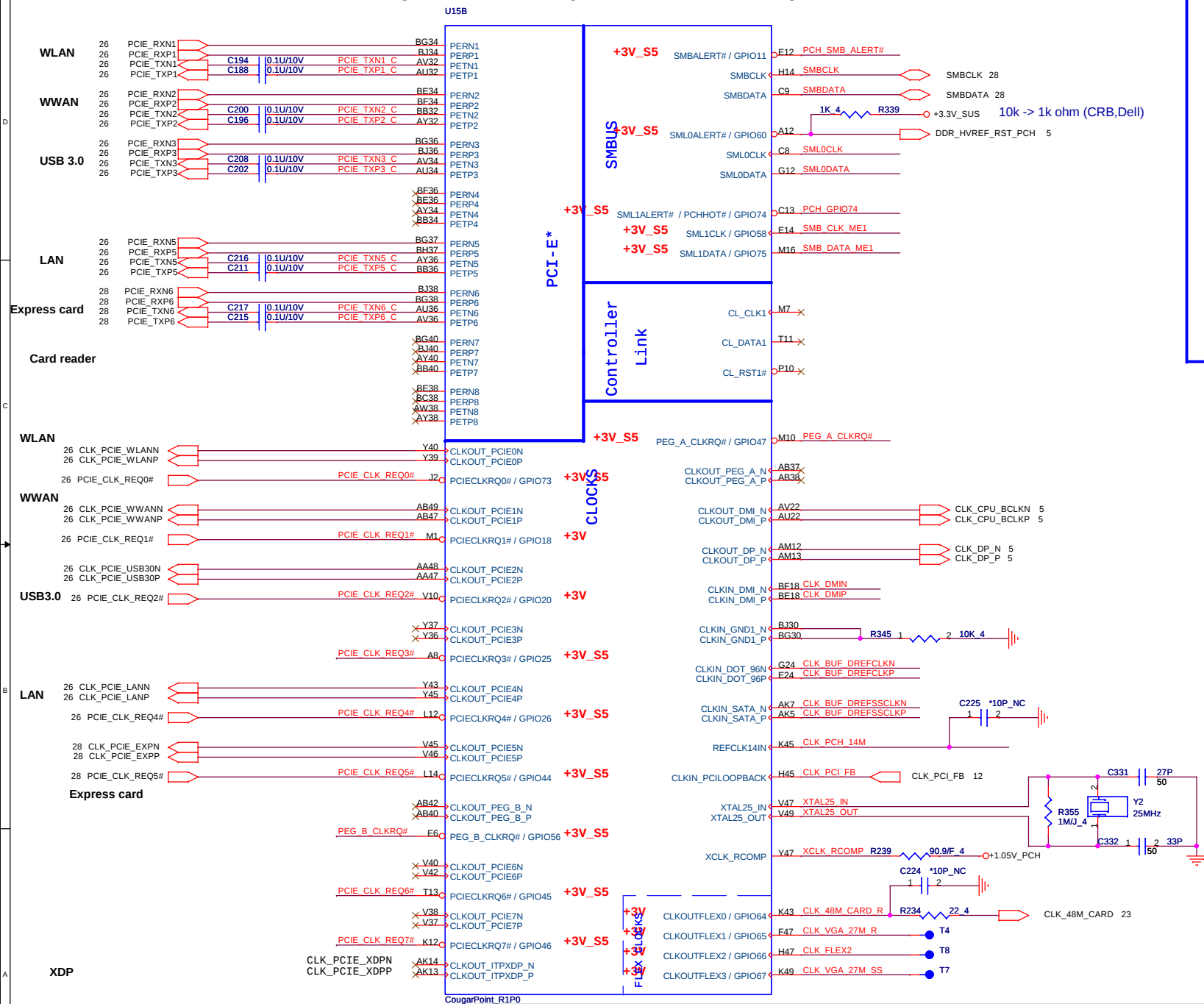
Take care while using GPIO19 for Hot Plug function

Move to Page12

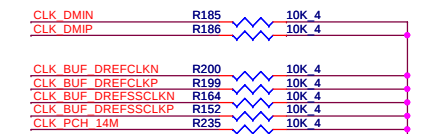
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS R146 *1K 4 NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R349 *1K 4 NC ACZ_SDO
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R181 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R212 1K 4 ACZ_SYNC_R

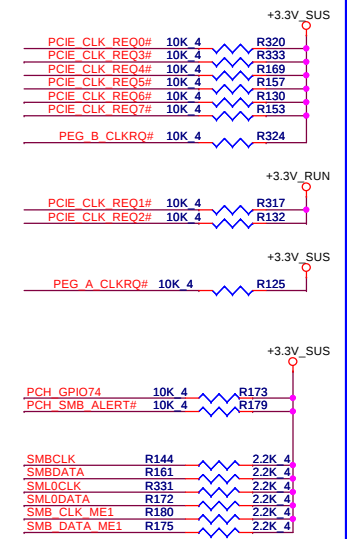
Cougar Point-M (PCI-E, SMBUS, CLK)



Stuff for Integrated CLK Gen Mode

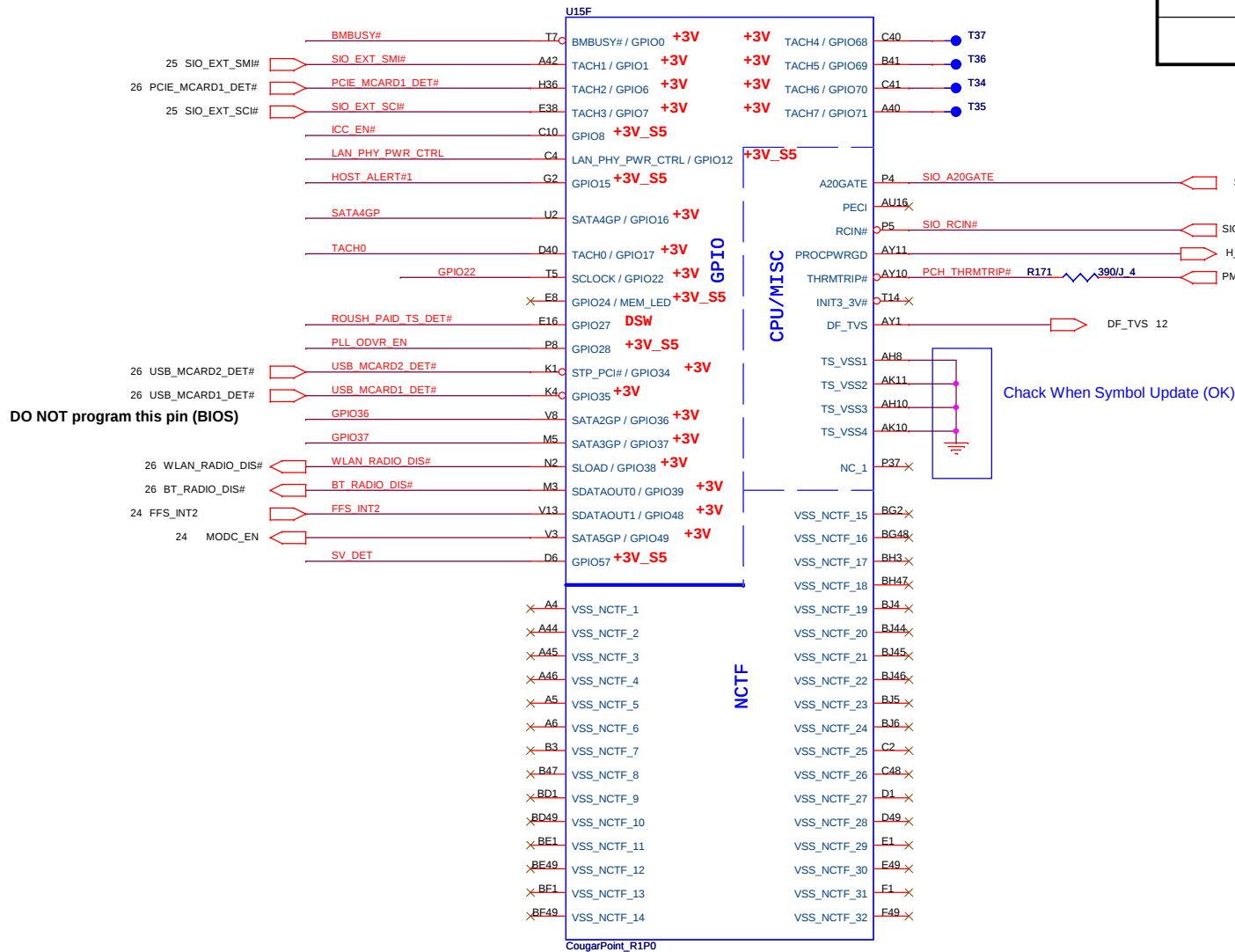


CLK_REQ/Strap Pin (CLG)

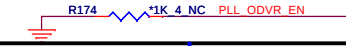


CougarPoint_R1P0	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 / GPIO64	• 33 / 27 / 48 / 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 / GPIO65	unsupported clock output value (Default) / 27 / 14.318 MHz output to SIO/EC / 48/24 MHz
CLKOUTFLEX2 / GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 / GPIO67	27/14.318 output to SIO/48/24 MHz (Default)

Cougar Point (GPIO, VSS_NCTF, RSVD)



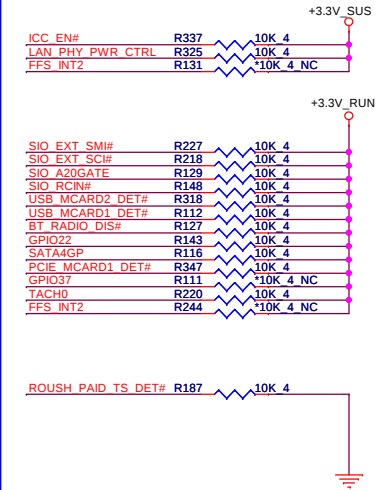
Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)



Ask Intel, what's the function?

Add Description in EC GPIO table (keyboard controller reset)

GPIO Pull-up/Pull-down(CLG)



Check When Symbol Update (OK)

Can be del



Have to Reserve

HOST_ALERT#1	R323	1K 4
Intel ME Crypto Transport Layer Security (TLS) cipher suite		
Low = Disable (Default)		
High = Enable		

MFG - TEST



SGPIO Confirm with Intel

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.



BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K FU and 100 ohm on this net for validation purpose.

DMI TERMINATION VOLTAGE OVERRIDE

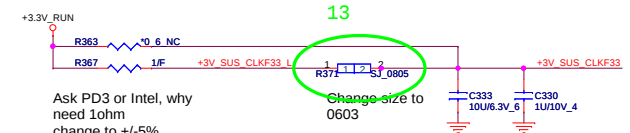
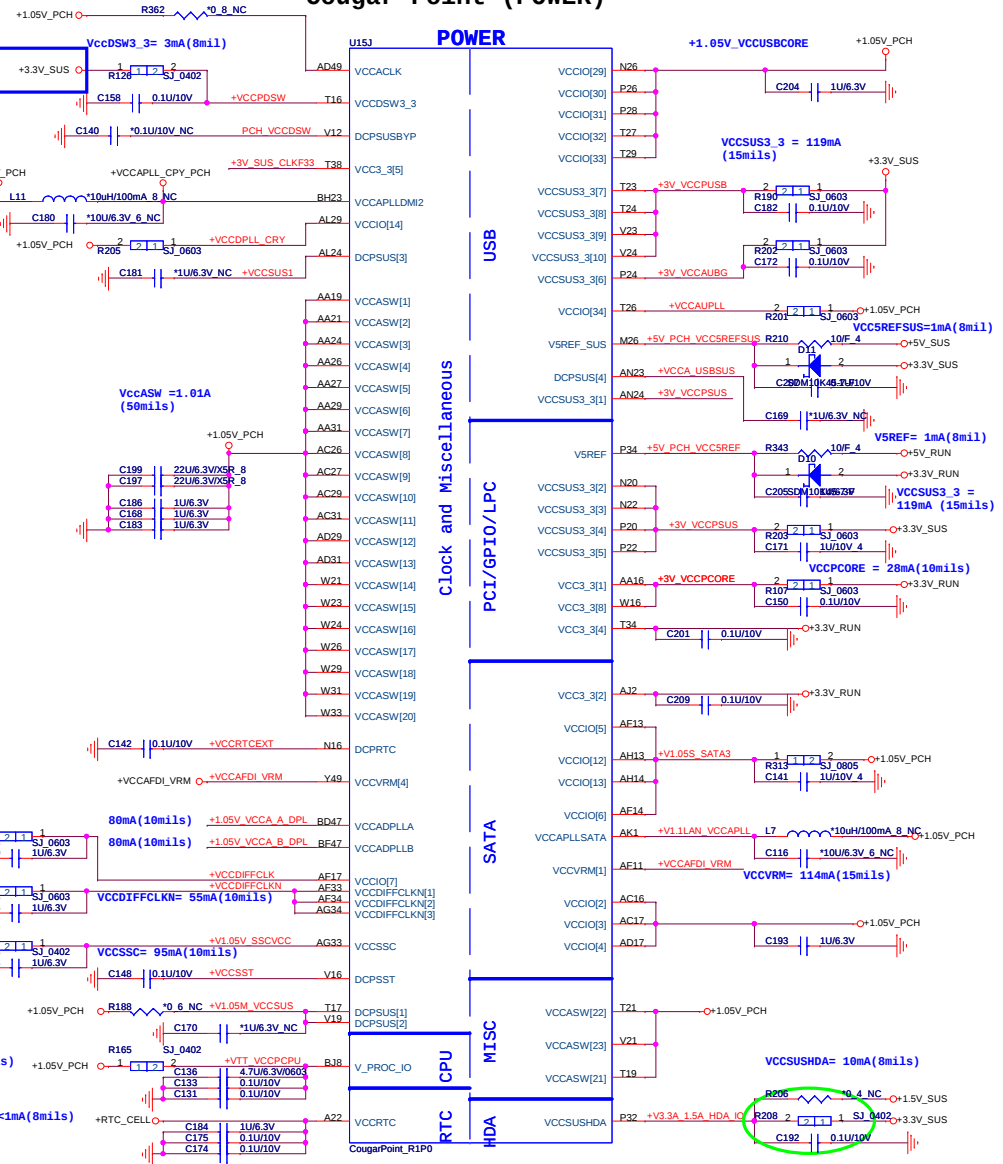
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



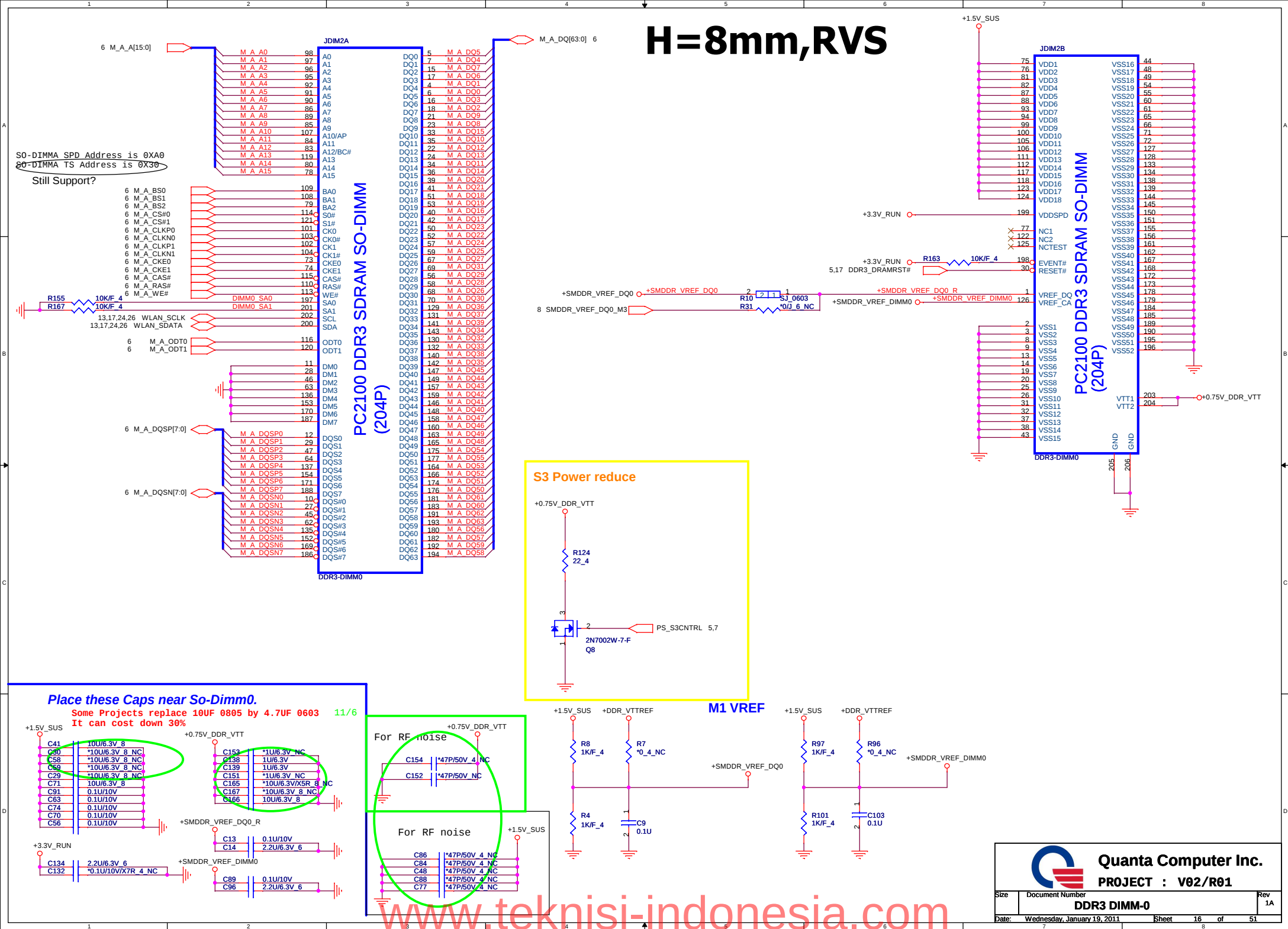
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PROJECT : V02/R01

Size	Document Number	Rev
	Cougar Point 6/7	1A
Date:	Wednesday, January 19, 2011	Sheet 14 of 51

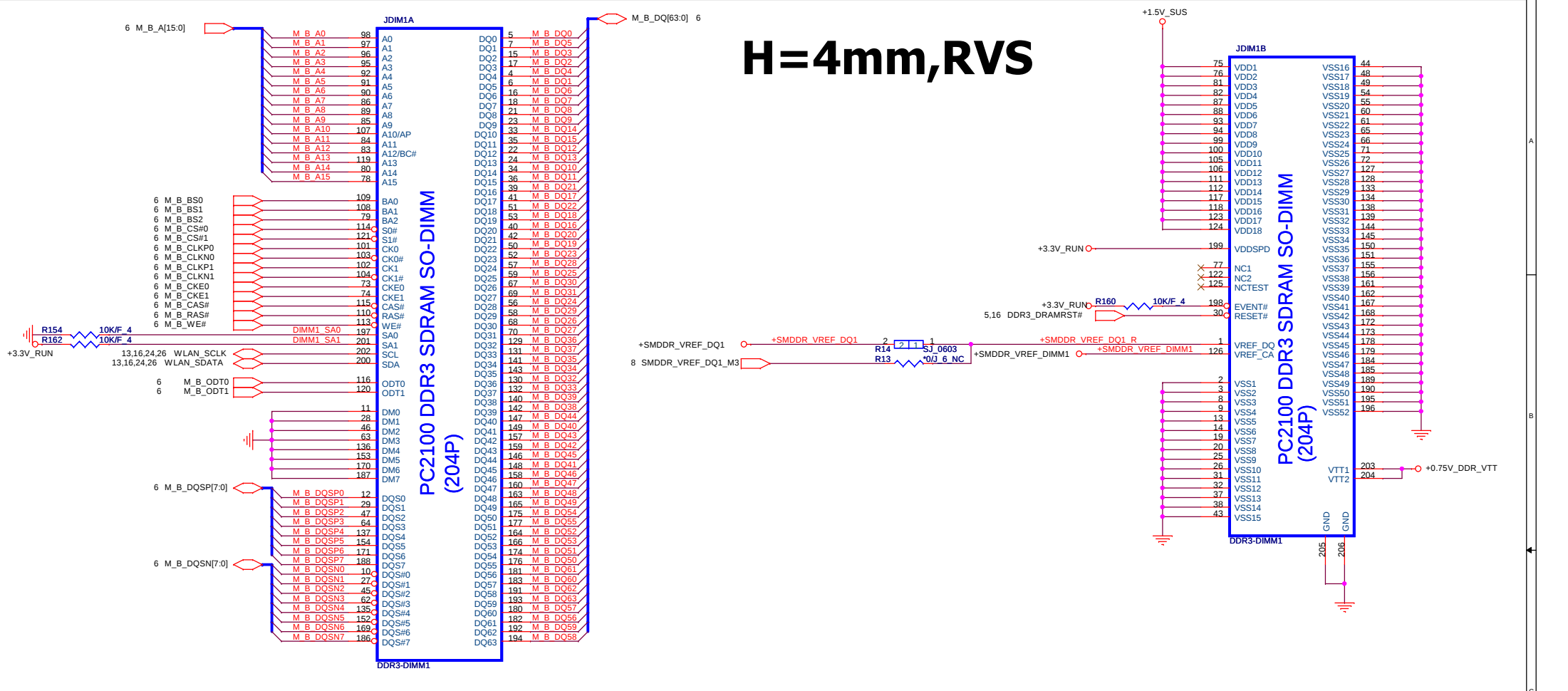
Cougar Point (POWER)

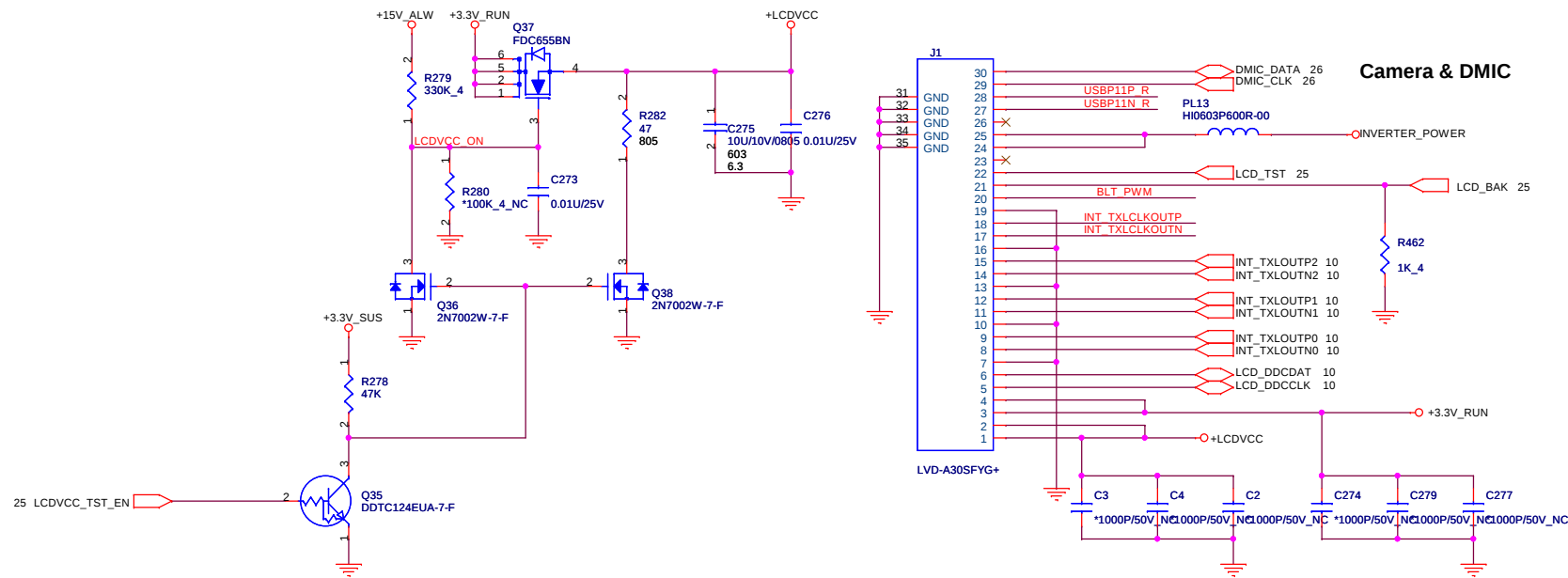


H=8mm,RVS

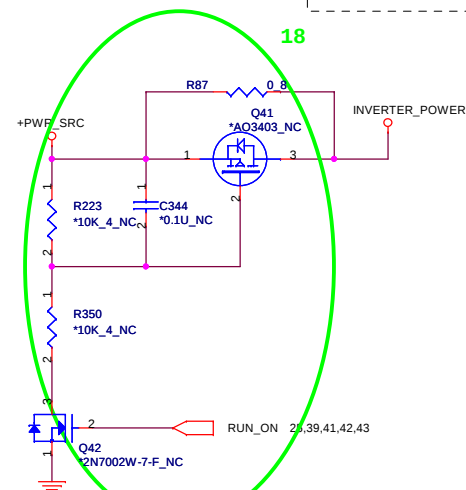
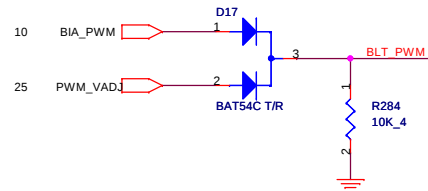
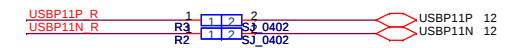
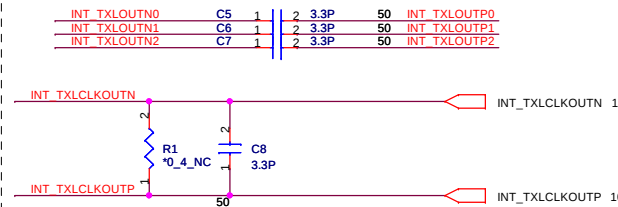


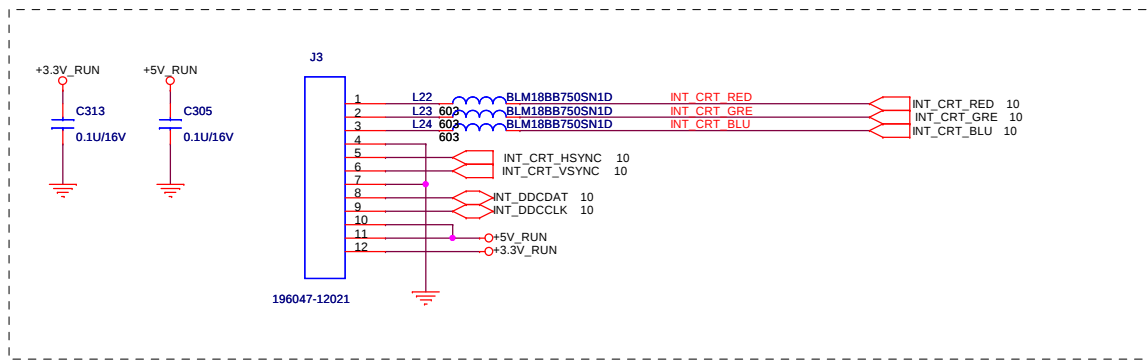
H=4mm,RVS



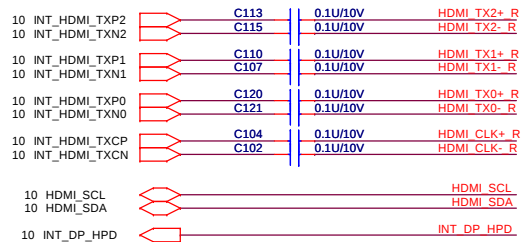


Shunt capacitors on LVDS for improving WWAN.

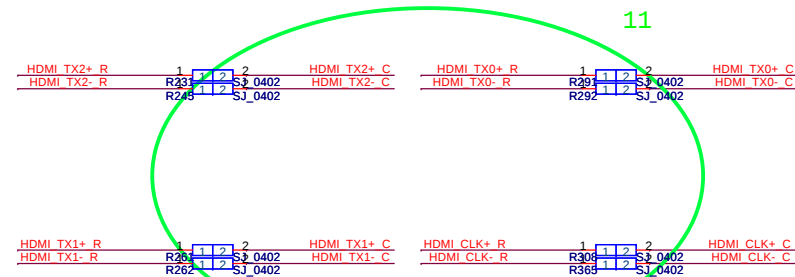




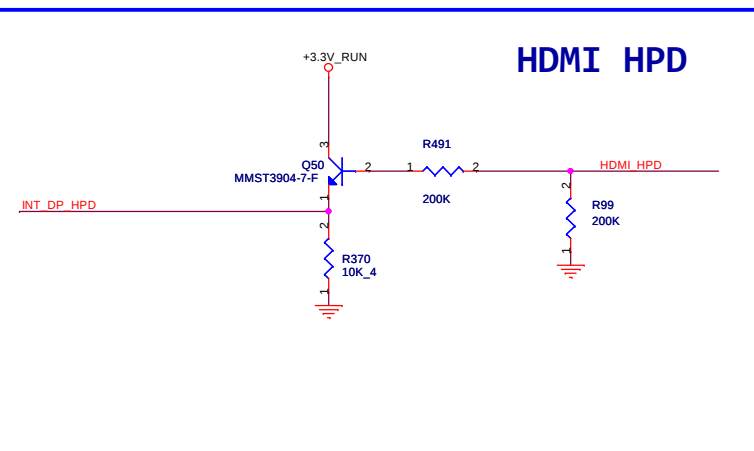
UMA HDMI



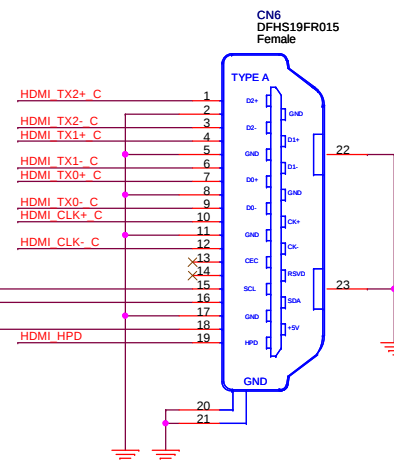
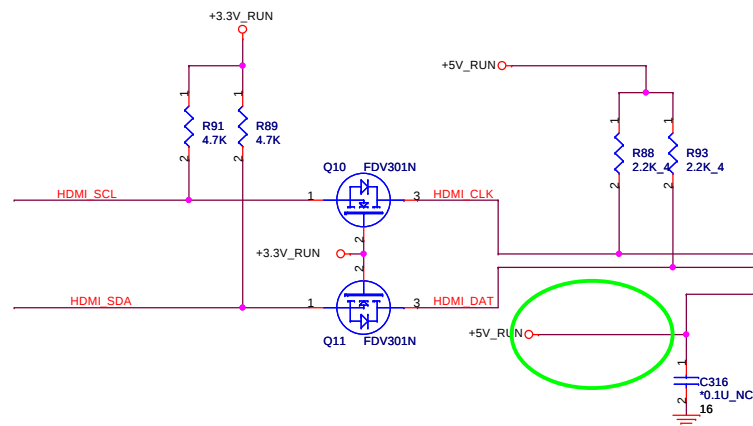
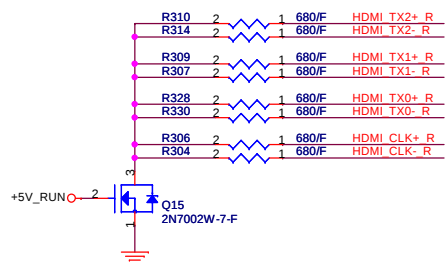
Reserve for EMI and close to HDMI CONN



HDMI HPD

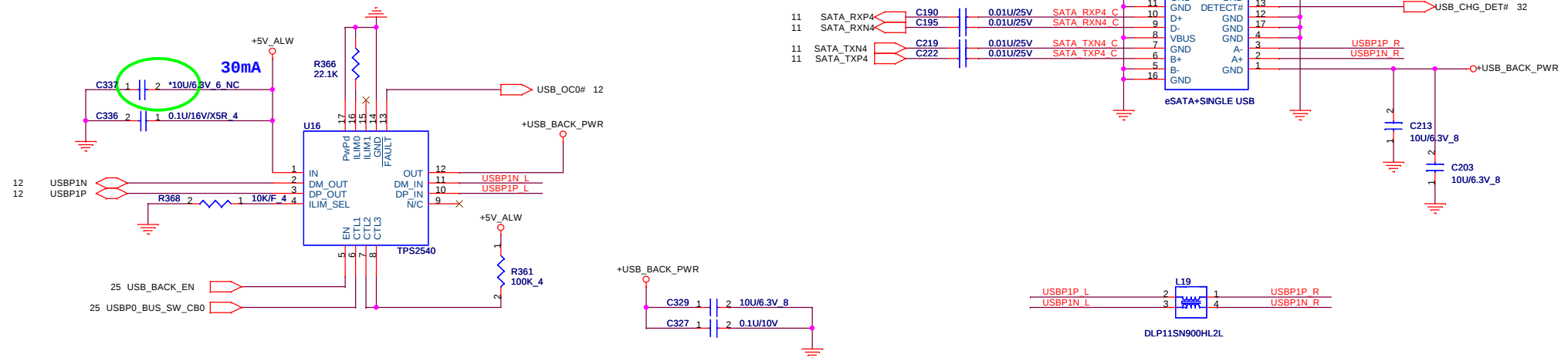


HDMI Conn.



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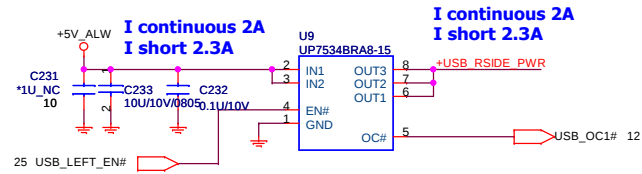
S3/S5 USB charging circuit



USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

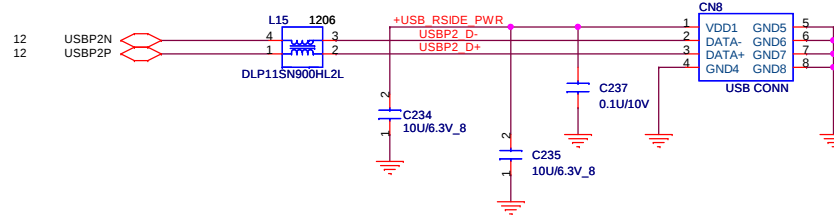
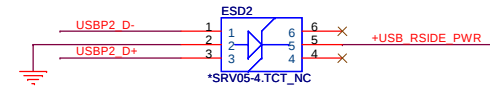
	R8224	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

UPI power switch

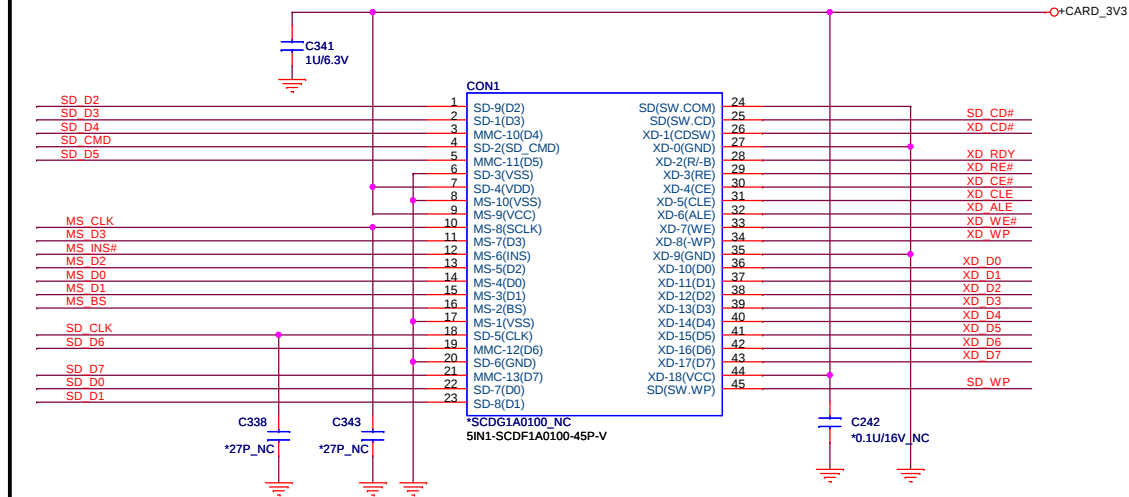


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

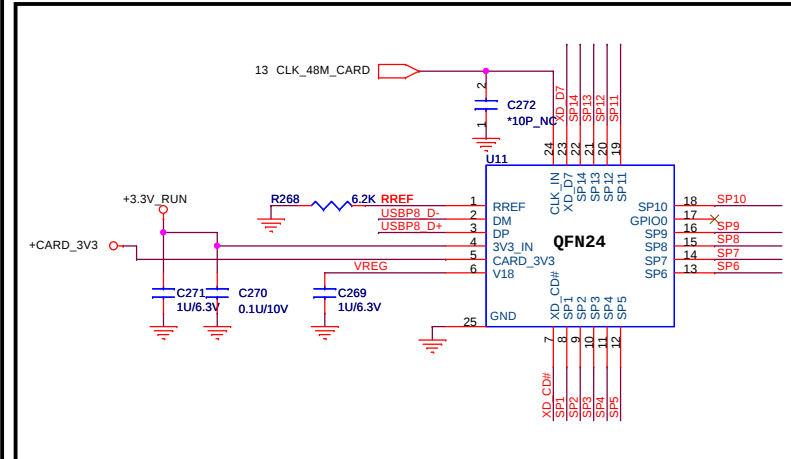
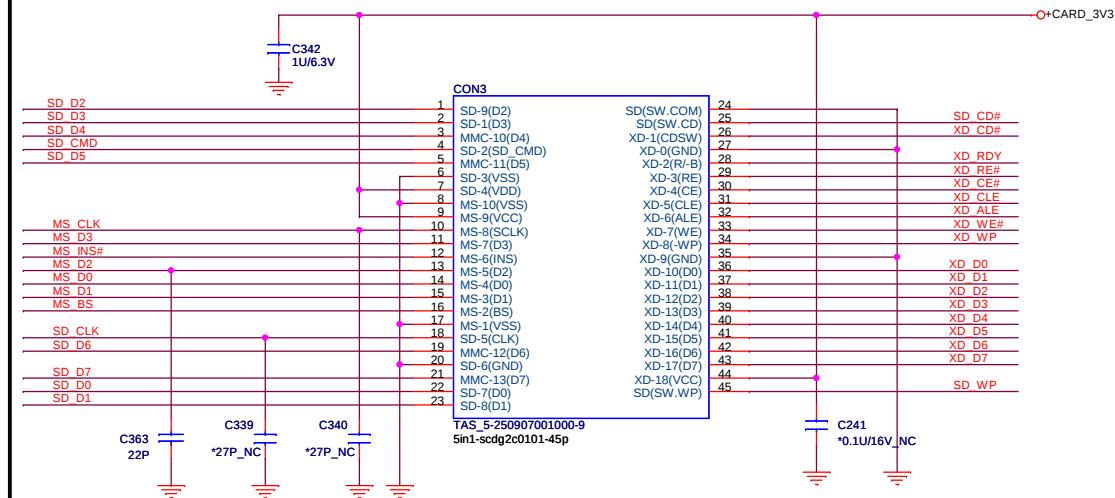
Place ESD diodes as close as USB connector.



Inspiron

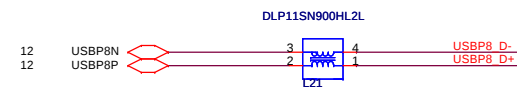


VOSTOR



SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#	SD D1	MS INS#
SP3	XD CE#	SD D0	MS D7
SP4	XD CLE	SD D7	MS D3
SP5	XD ALE	SD CD#	MS D6
SP6	XD WE#	SD D6	MS D2
SP7	XD WP	SD D5	MS D0
SP8	XD D0	SD D4	MS D4
SP9	XD D1	SD D3	MS D1
SP10	XD D2	SD D2	MS D5
SP11	XD D3	SD D1	MS BS
SP12	XD D4	SD D0	
SP13	XD D5	SD D7	
SP14	XD D6	SD D6	

Share Pin



Cardreader	POP	NC
Inspiron	CON1	CON3
VOSTOR	CON3	CON1

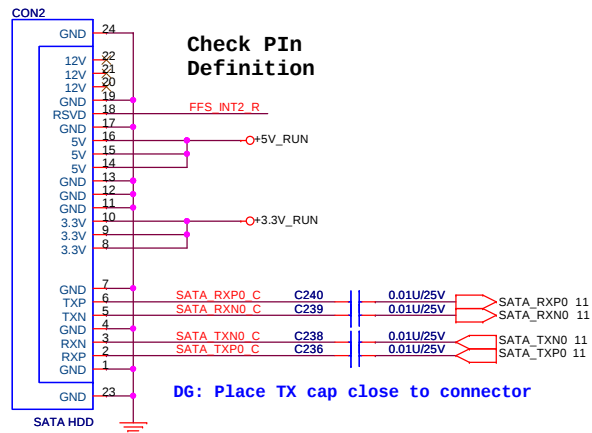


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PROJECT : V02/R01

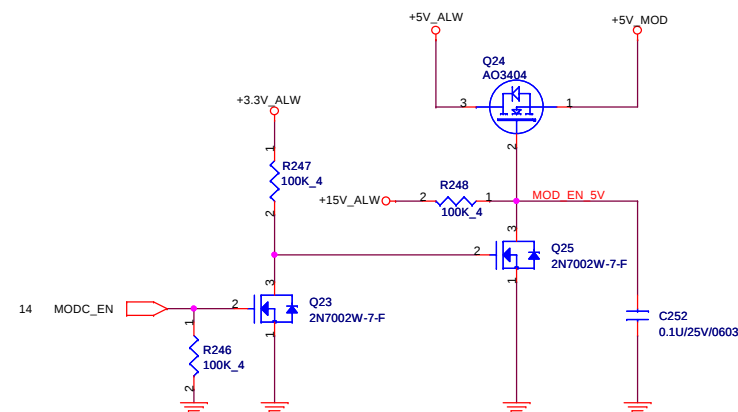
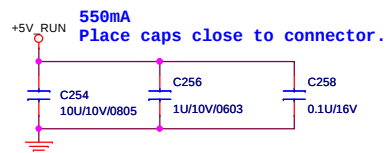
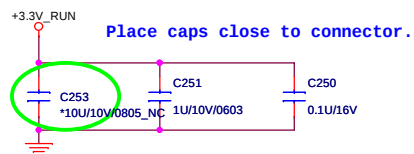
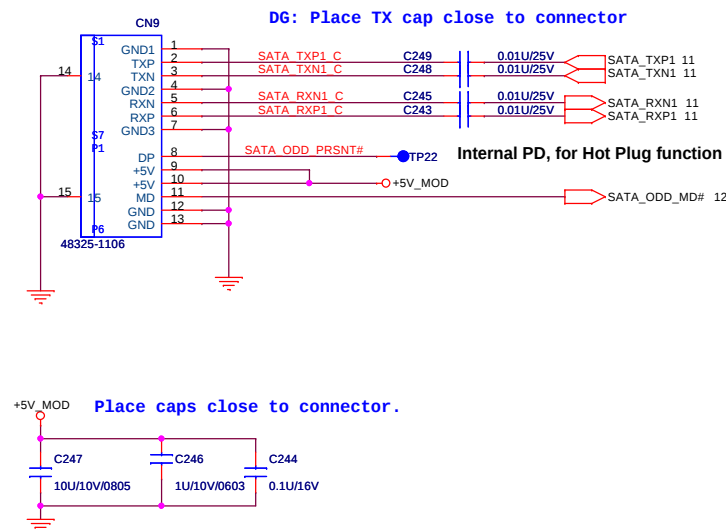
Size	Document Number	Rev
	Cardreader (RTS5128)	1A
Date	Wednesday, January 19, 2011	Sheet 23 of 51

SATA Connector

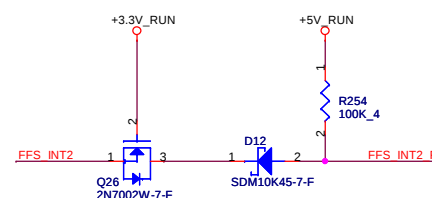
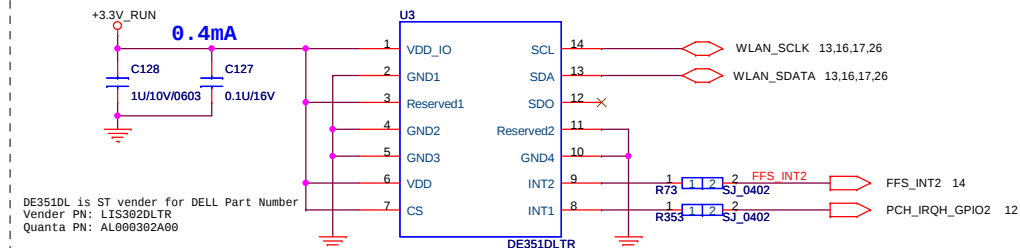
UM8



ODD Connector



3-axis Fall Sensor (HDD data protector)

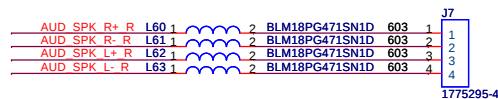
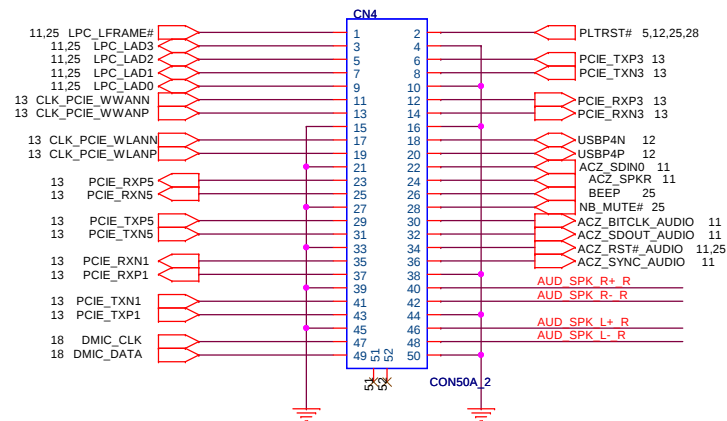
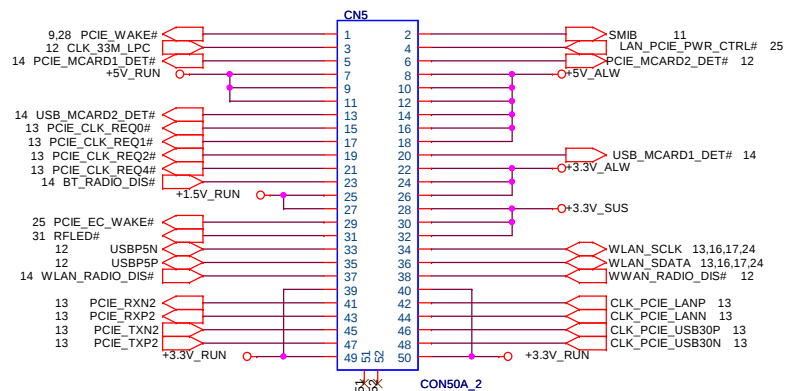


3-axis Fall Sensor	V08TOR	Inspiron
U3, Q26, D12 R73, R254, R353 C127, C128	POP	NC



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PROJECT : V02/R01

Size	Document Number	Rev
	SATA HDD/ODD	1A
Date:	Wednesday, January 19, 2011	Sheet 24 of 51

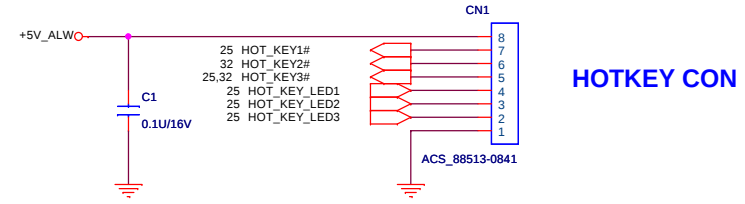
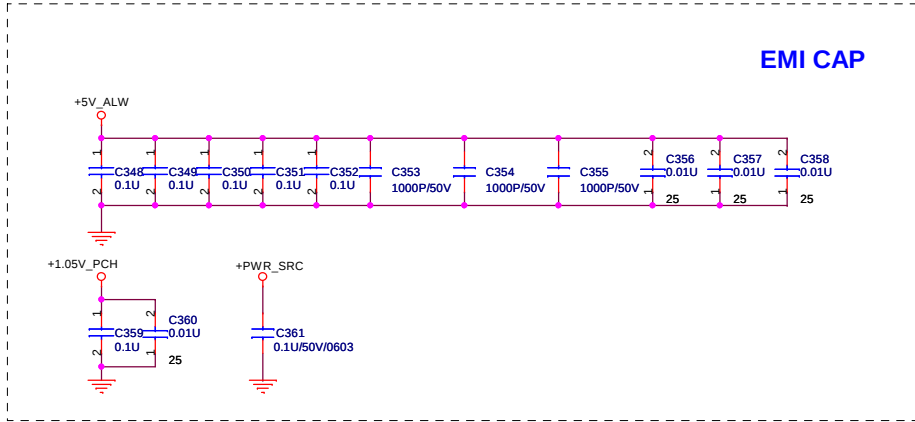


Int. Stereo Speakers
5V / 4 Ohm / 2W

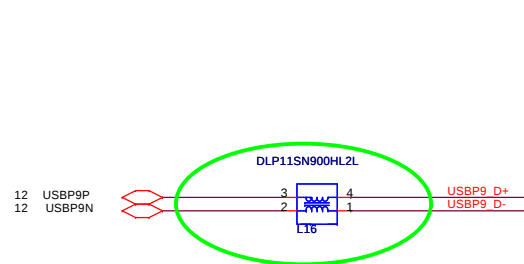


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PROJECT : V02/R01

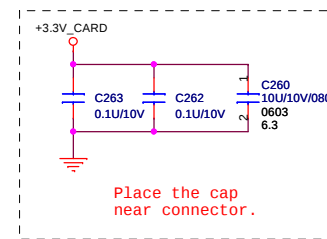
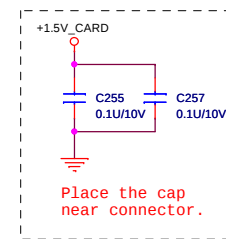
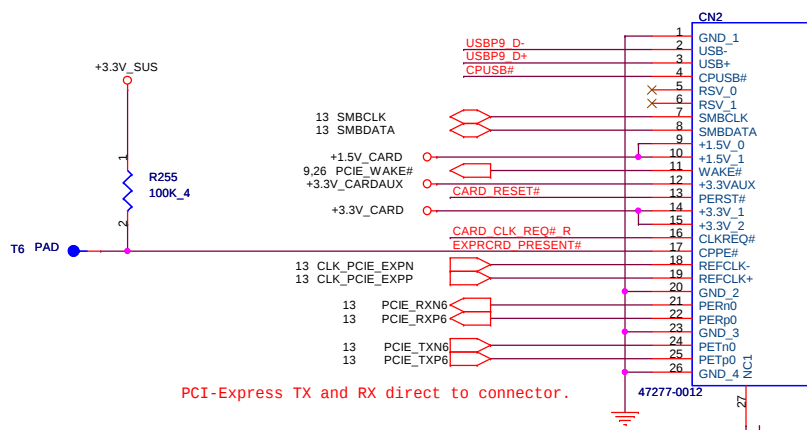
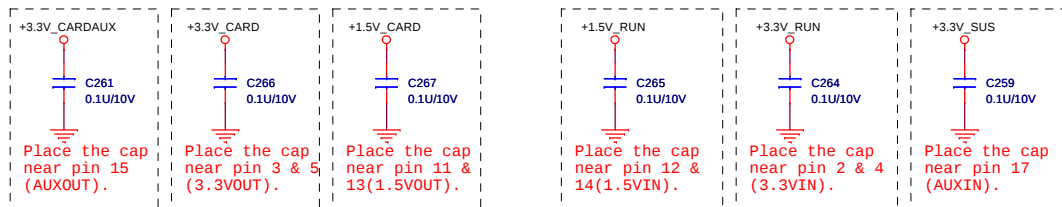
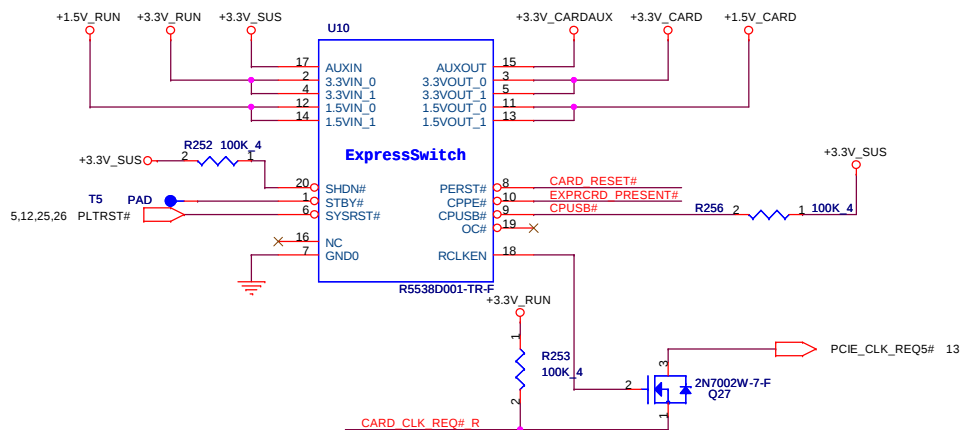
Size	Document Number	Rev
	SIO (ITE8518E)	1A
Date:	Wednesday, January 19, 2011	Sheet 26 of 51



Express Card



+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



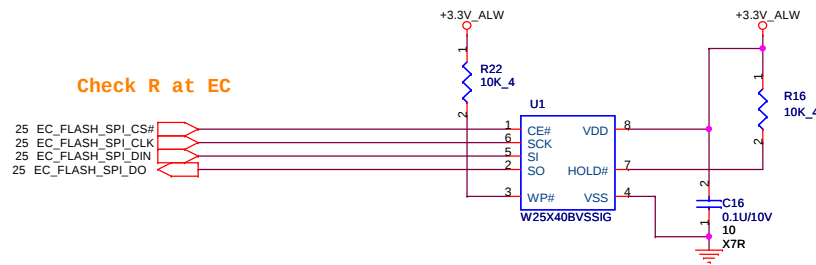
If close enough, could combine



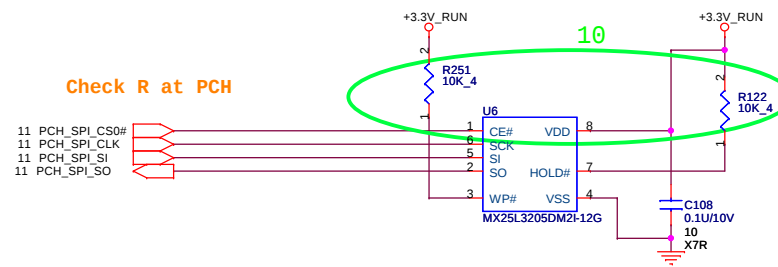
Quanta Computer Inc.
PROJECT : V02/R01

Size	Document Number	Rev
	LAN (RTL8111EL)	1A
Date:	Wednesday, January 19, 2011	Sheet 28 of 51

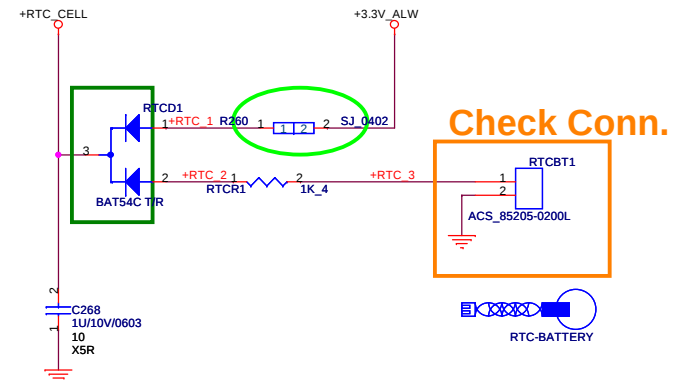
For EC 4Mbit (512K Byte)



For PCH 32Mbit (4M Byte)



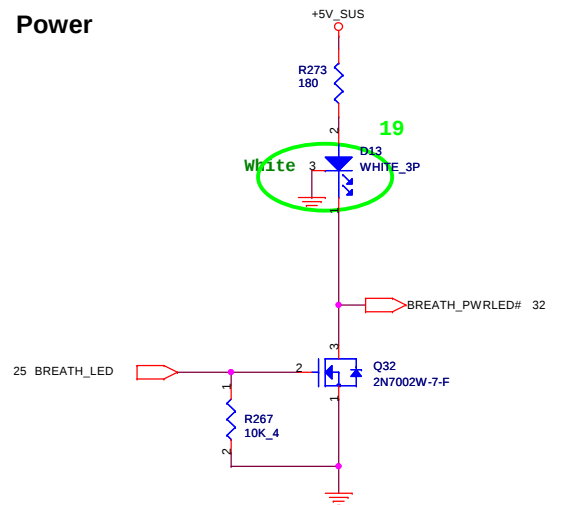
RTC



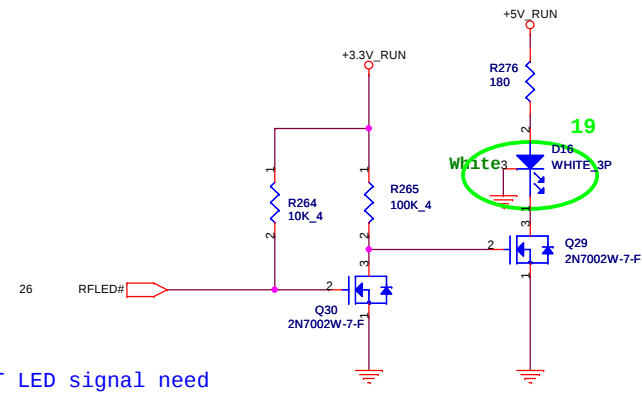
Double, 25°C, Vf=0.4V, If=25mA
one, 25°C, Vf=0.35V, If=15.8mA



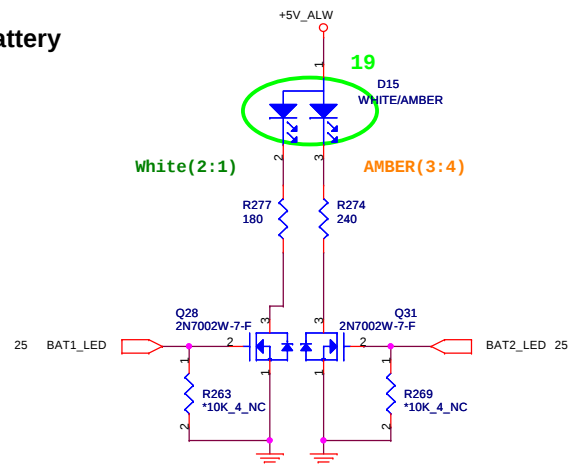
Power



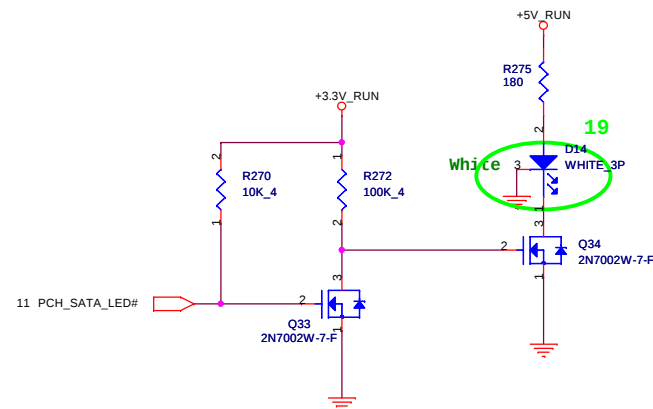
Bluetooth / WLAN on/off LED



Battery

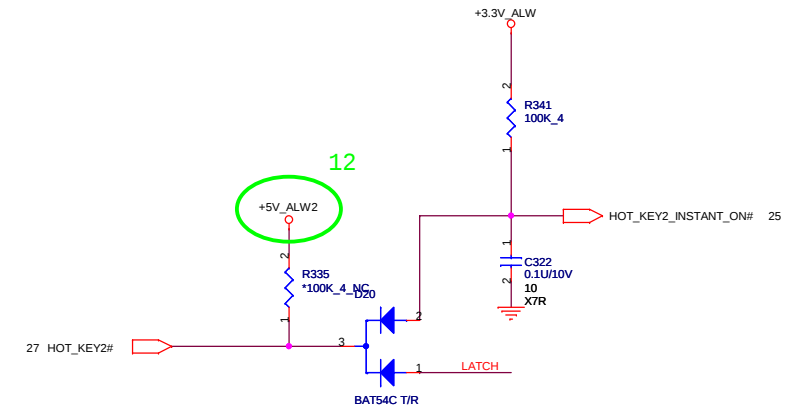
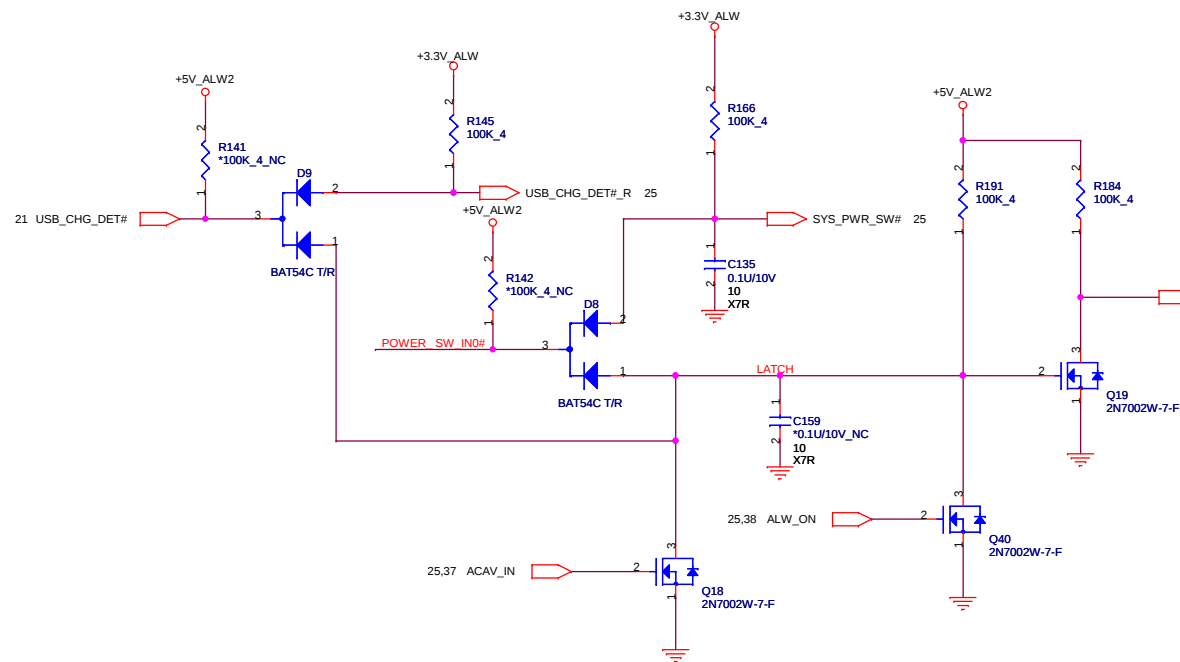


HDD activity LED.



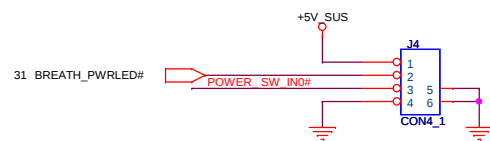
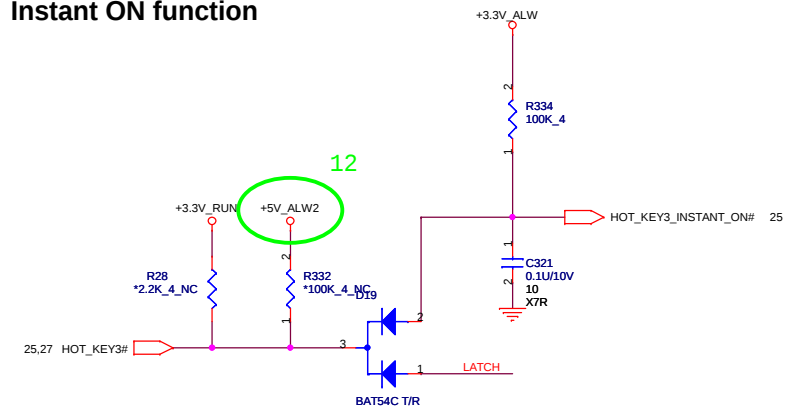
VOSTOR	R273, R276, R277, R275	R274
	180 ohm PN:CS11802JB15	240ohm PN:CS12402JB13
Inspiron	R273, R276, R277, R275	R274
	390 ohm PN:CS13902JB14	330 ohm PN:CS13302JB21

3VALW ON POWER LOGIC



Vostro pop D19,C321,R334 depop R28,R30
Inspiron depop D19,C321,R334 pop R28,R30

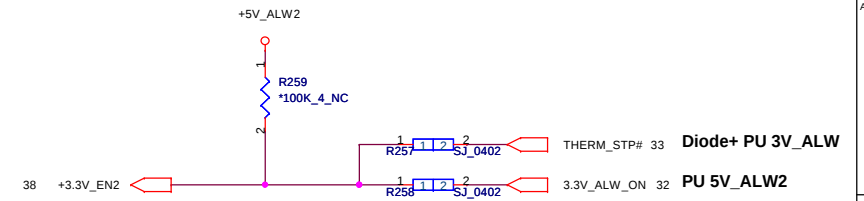
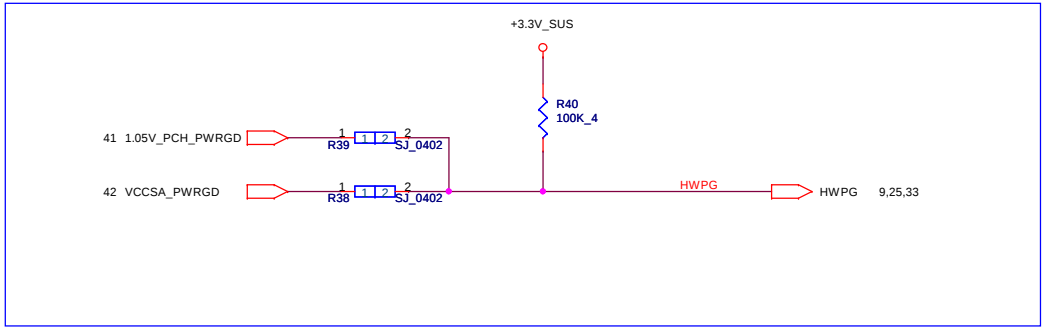
Instant ON function

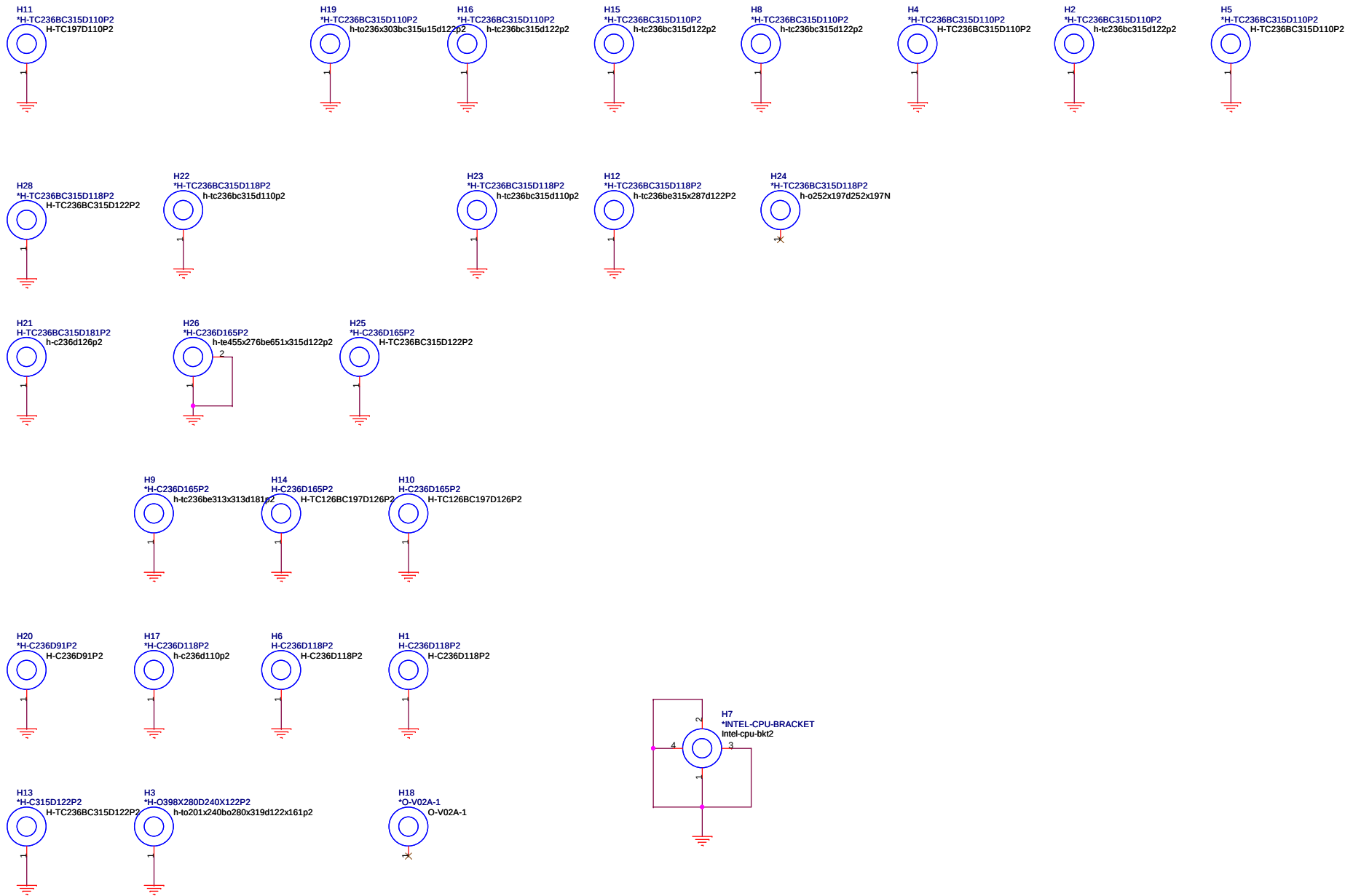


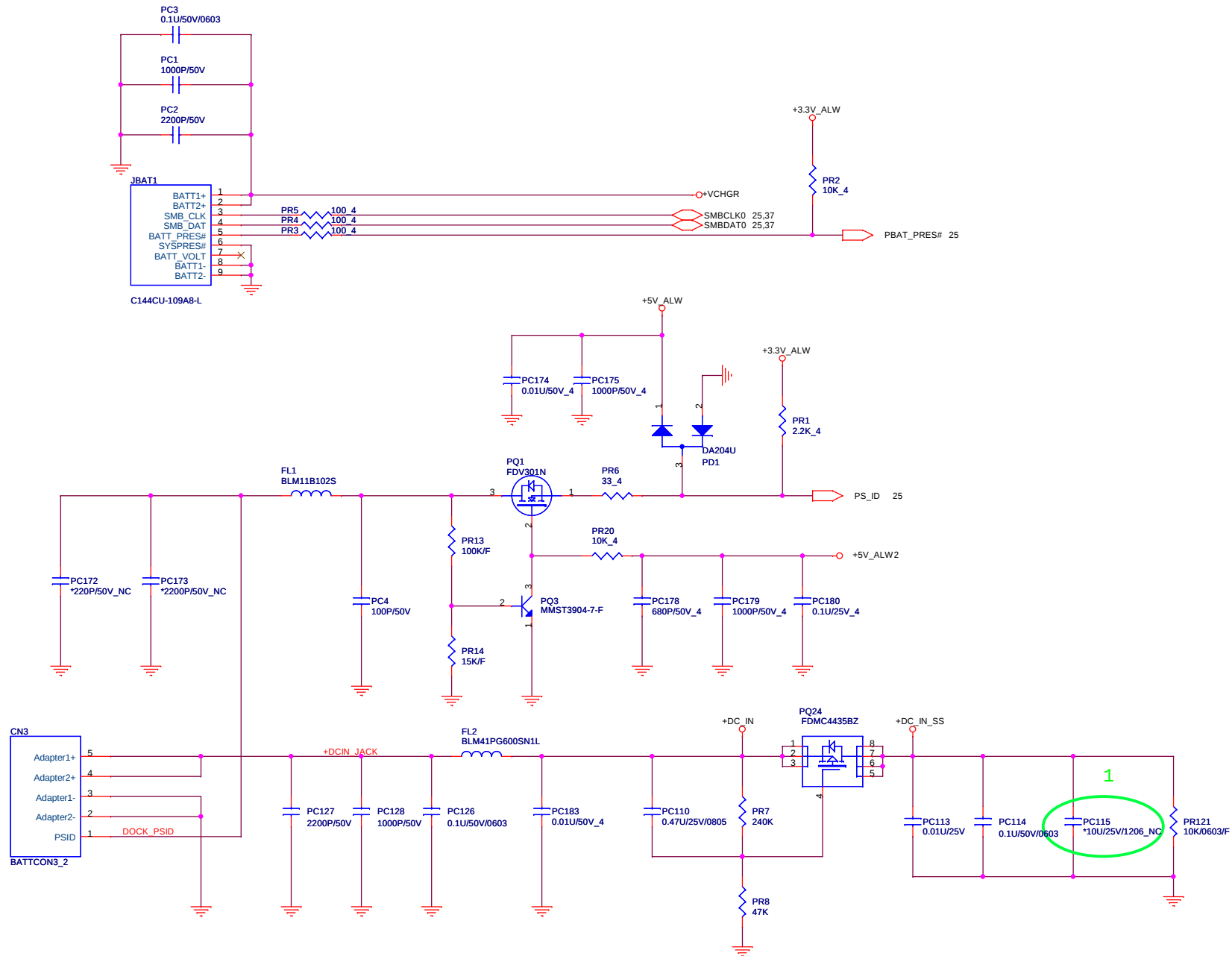
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Size	Document Number	Rev
	FAN & THERMAL	1A
Date:	Wednesday, January 19, 2011	Sheet 33 of 51







Quanta Computer Inc.
PROJECT : V02/R01

Size	Document Number	Rev
	DC IN / BATT	1A
Date:	Wednesday, January 19, 2011	Sheet 36 of 51

